

Compal confidential

Schematics Document

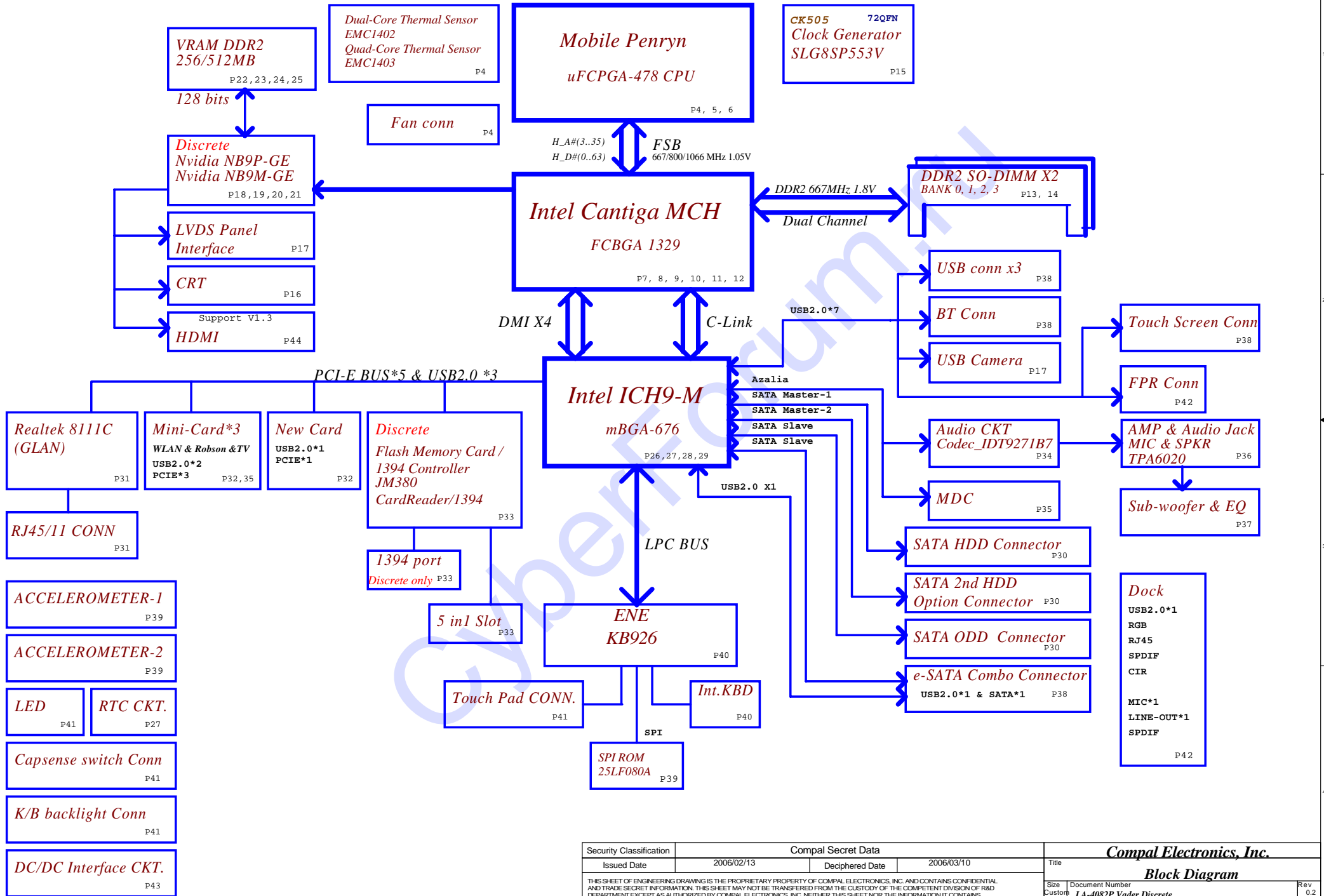
Mobile Penryn uFCPGA with Intel
Cantiga_PM+ICH9-M core logic

LA-4082P Vader Discrete (NB9P-GS,NB9M-GE)

2008-04-23 Rev 1.0

Security Classification	Compal Secret Data			Title <i>Compal Electronics, Inc.</i>		
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Cover Sheet		
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Montevina Consumer Discrete



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Voltage Rails O MEANS ON X MEANS OFF

power plane State				+5VS +3VS +1.5VS +0.9V +VCCP +CPU_CORE +VGA_CORE +2.5VS +1.8VS +1.2VS +0.9VGA
	+B	+5VALW +3VALW	+1.8V	
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBus Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	Thermal Sensor	SODIMM	CLK CHIP	MINI CARD	LCD	Sensor board
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	V
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X	X
DDC2_CLK DDC2_DATA	NB9M	X	X	X	X	X	X	X	V	X

USB

assignment:

- USB-0 Right side
- USB-1 Right side
- USB-2 Left side(with ESATA)
- USB-3 Dock
- USB-4 Camera
- USB-5 WLAN
- USB-6 Bluetooth
- USB-7 Finger Printer
- USB-8 MiniCard(WWAN/TV)
- USB-9 Express
- USB-10 X
- USB-11 X

PCIe

assignment:

- PCIe-1 TV tuner/WWAN/Robeson
- PCIe-2 X
- PCIe-3 WLAN
- PCIe-4 New Card
- PCIe-5 Card
- PCIe-6 GLAN (Marvell)

Symbol Note :

- : means Digital Ground
- : means Analog Ground

- @ : means just reserve , no build
- DEBUG@ : means just reserve for debug.

EC SM Bus1 address

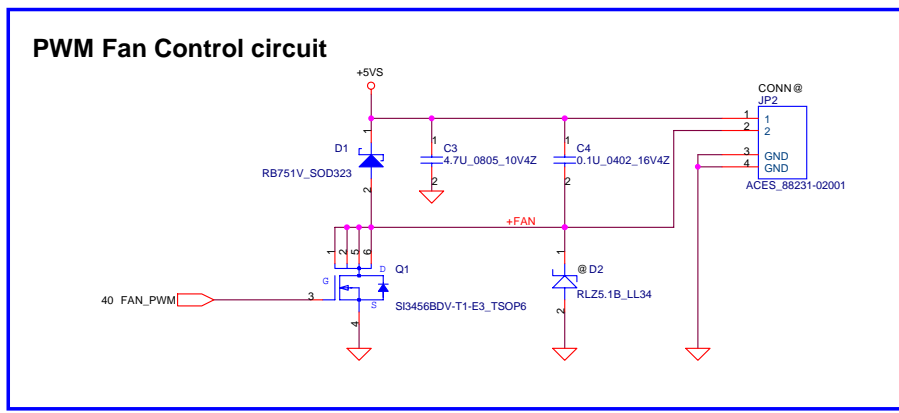
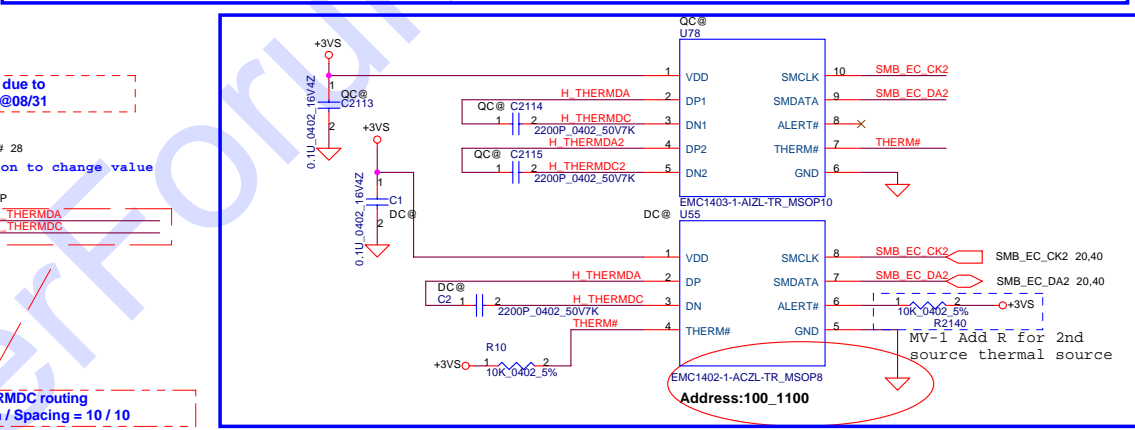
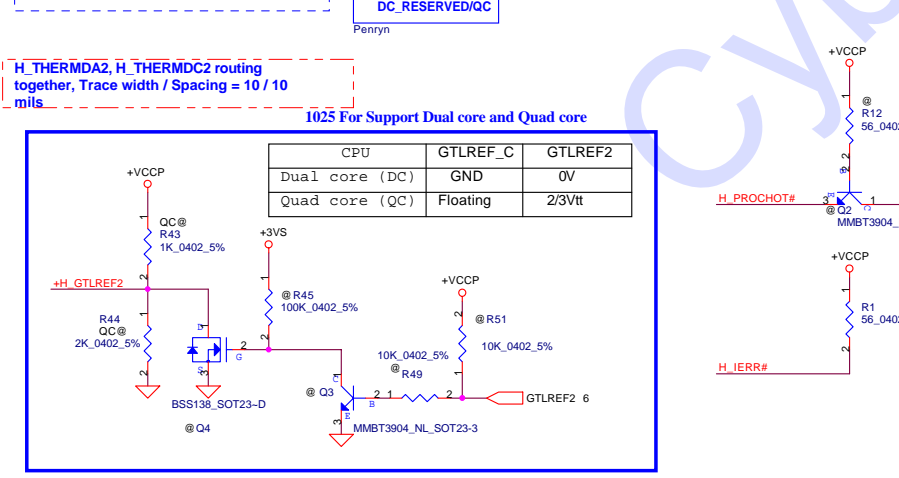
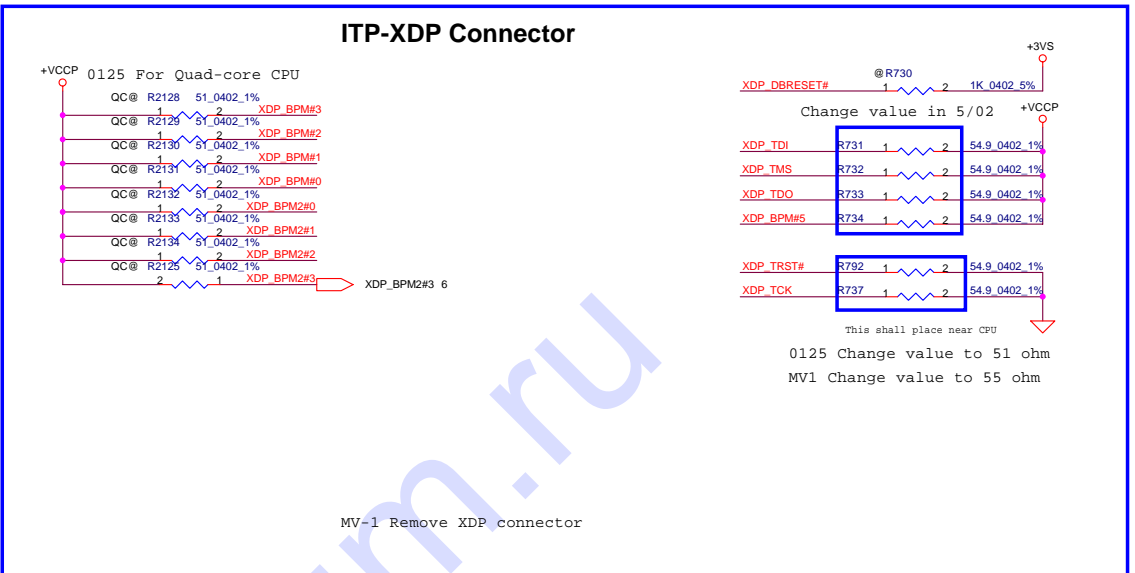
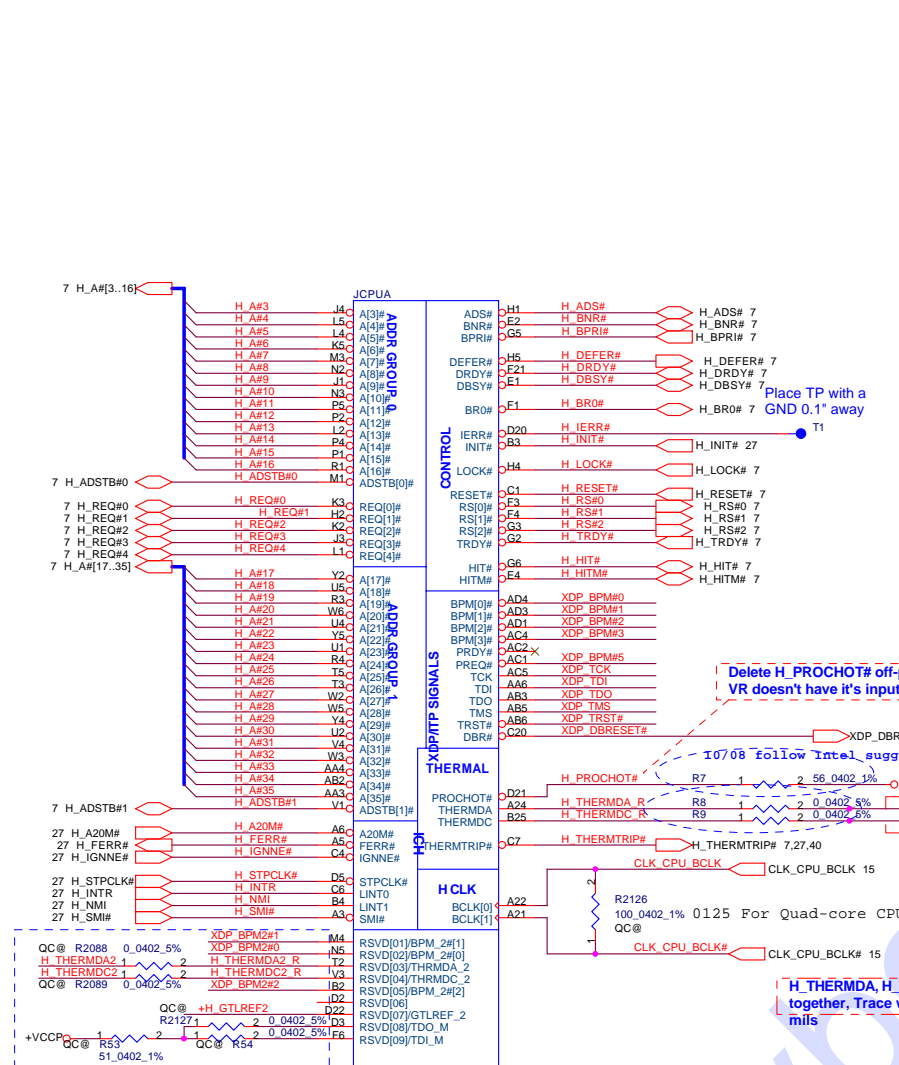
EC SM Bus2 address

Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 011X	CPU EMC1402	4CH	1001 1000b
24C16	A0H	1010 000X	VGA	4DH	1001 1010b
CAP BOARD – Cypress	38H				
CAP BOARD – ST	b0H				
G-sensor		0011 1001(read) 0011 1010(write)			

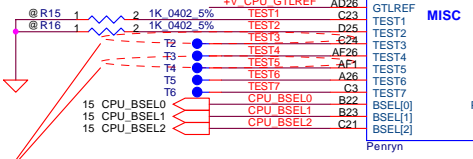
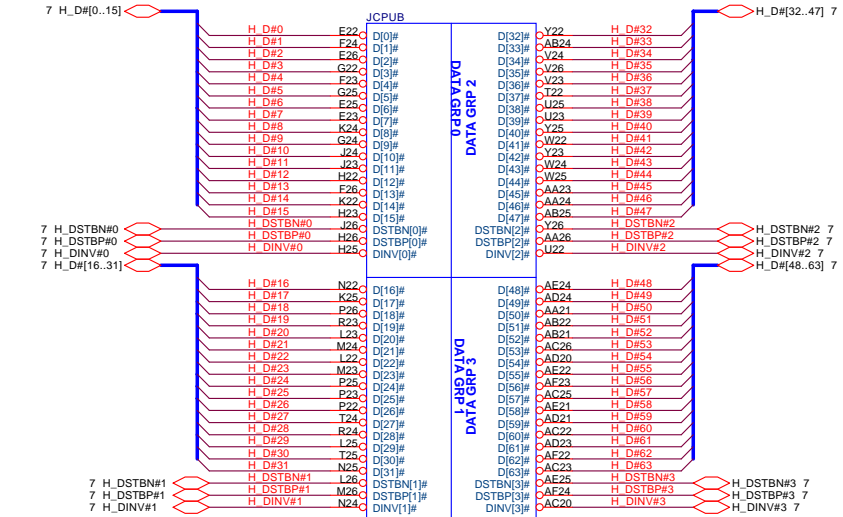
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

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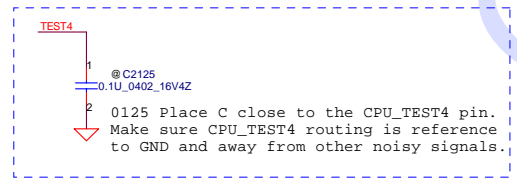
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2006/02/13	Deciphered Date	2006/03/10	Penryn(1/3)-AGTL+/ITP-XDP	
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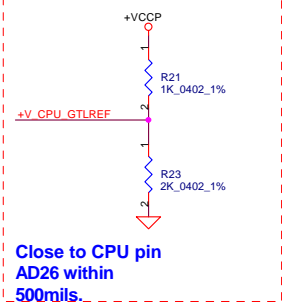
* Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

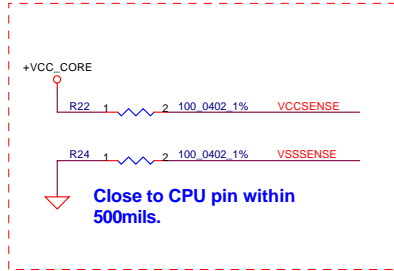


0125 Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signals.



Close to CPU pin AD26 within 500mils.

Length match within 25 mils. The trace width/space/other is 20/7/25.

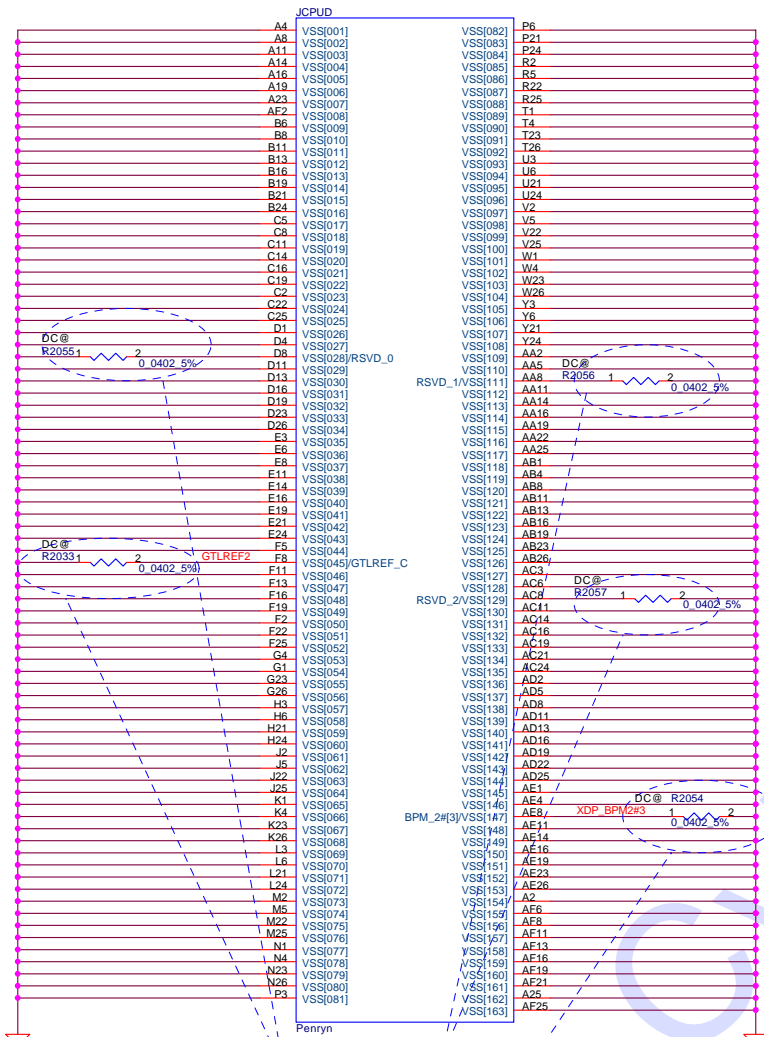


Close to CPU pin within 500mils.

1025 For Support Dual core and Quad core

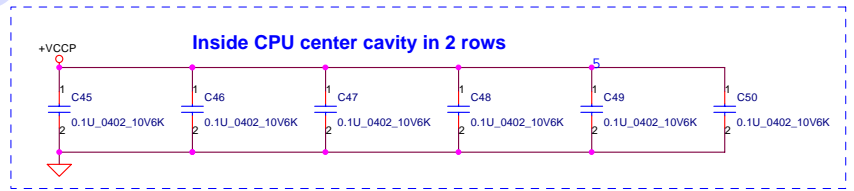
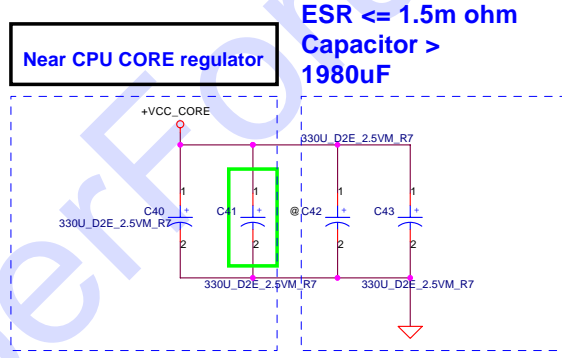
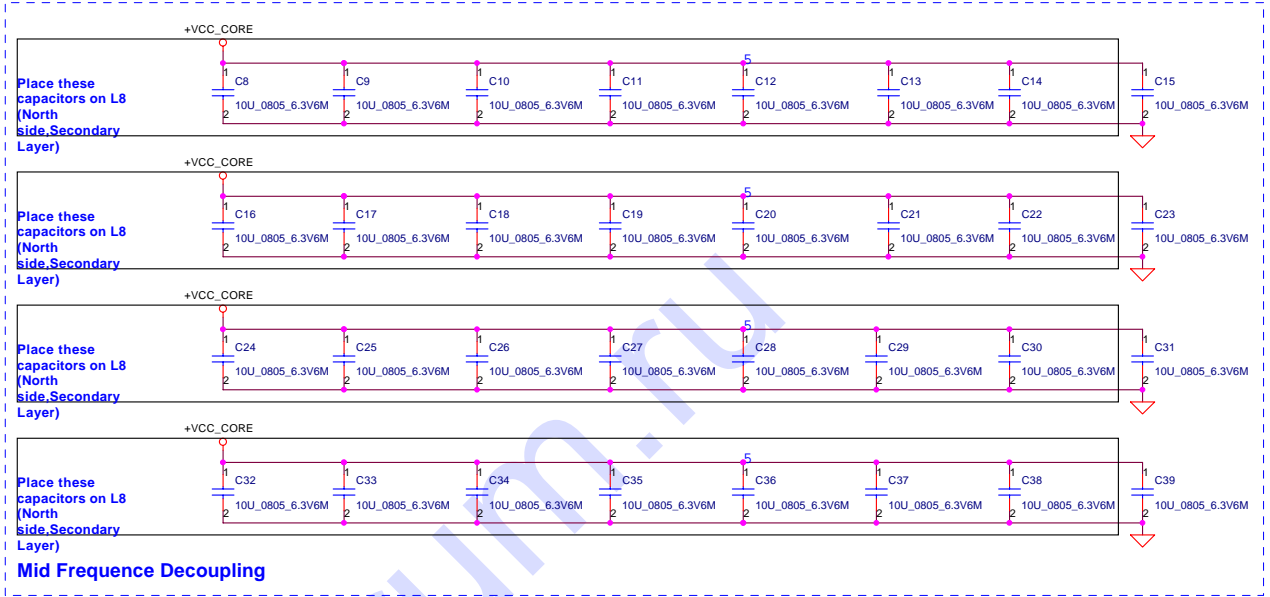
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Penryn(2/3)-AGTL+/ITP-XDP		
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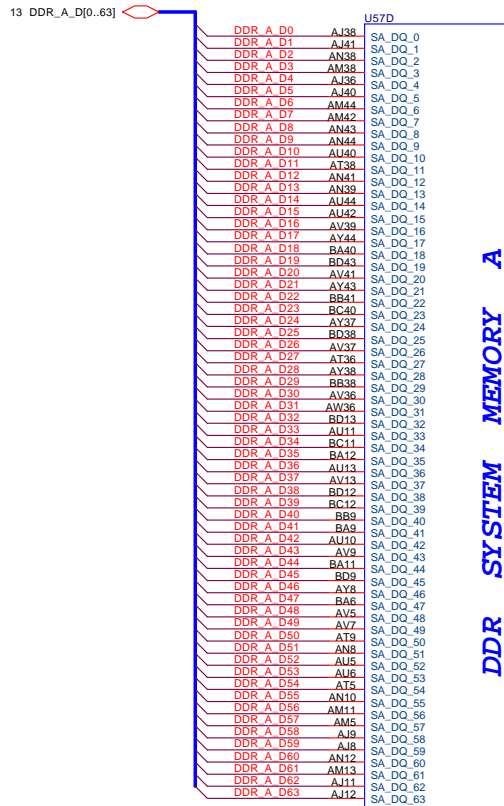


1025 For Support Dual core and Quad core

- GTLREF2 → GTLREF2 4
- XDP_BPM2#3 → XDP_BPM2#3 4

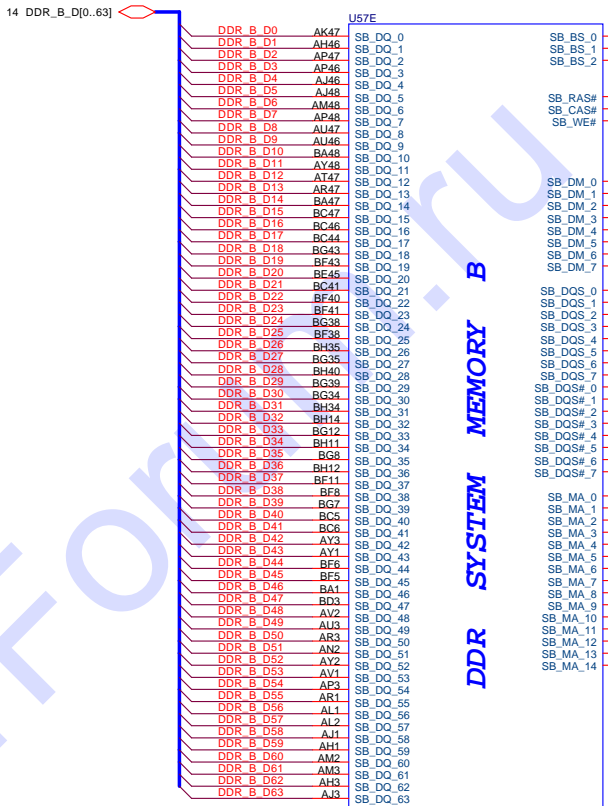


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CANTIGA ES_FCBGA1329

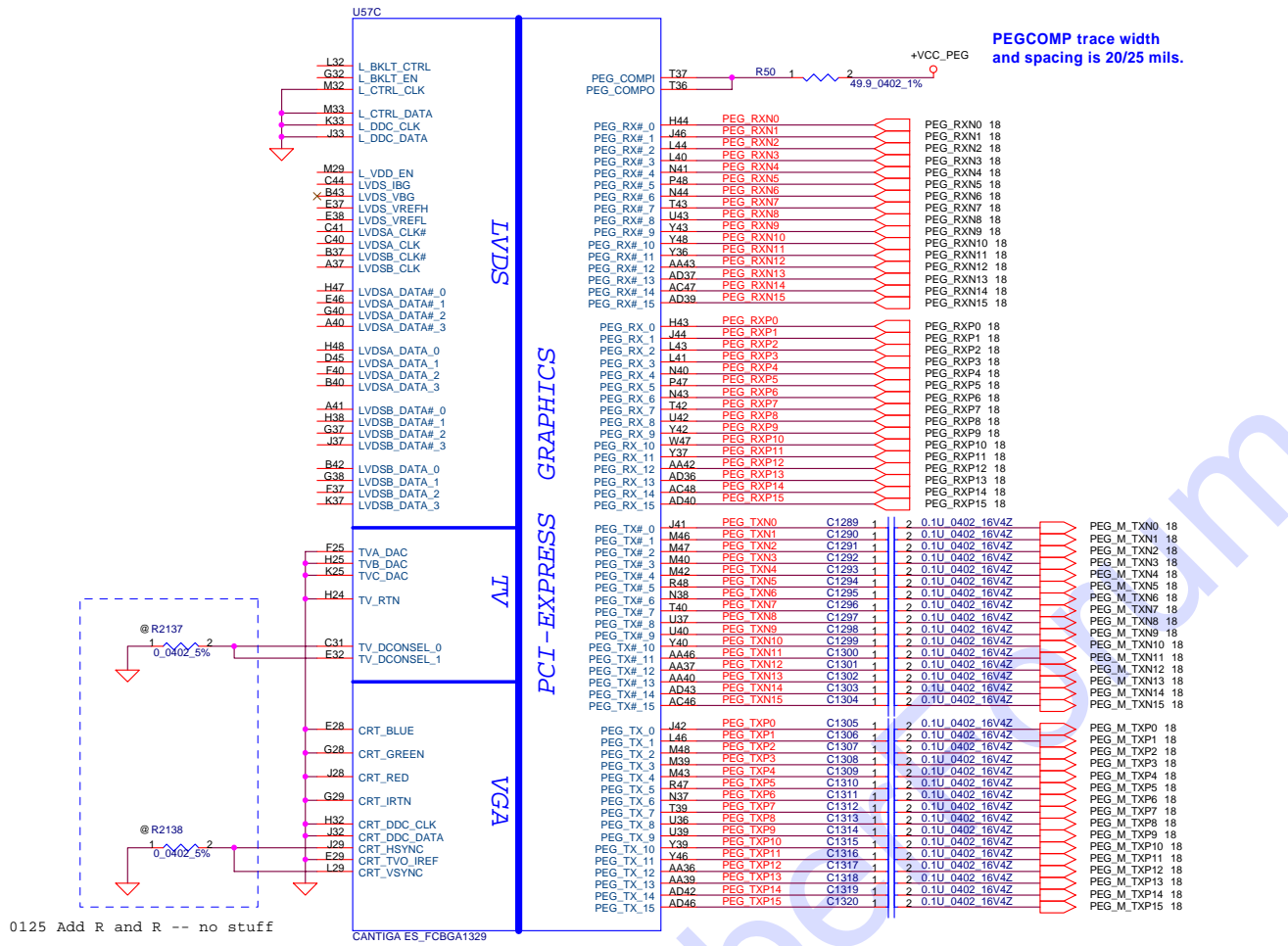
DDR SYSTEM MEMORY A



CANTIGA ES_FCBGA1329

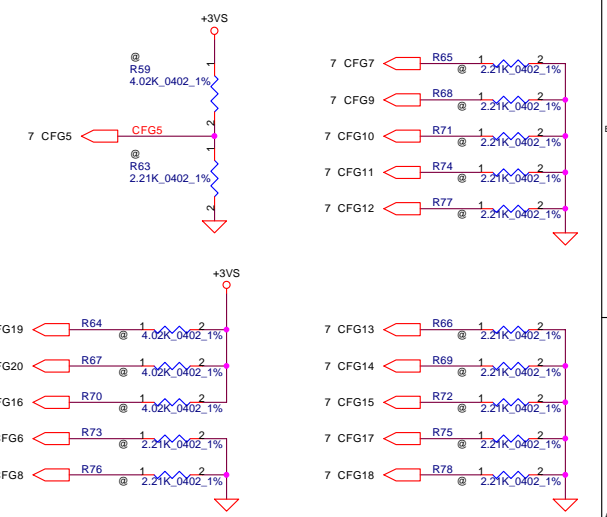
DDR SYSTEM MEMORY B

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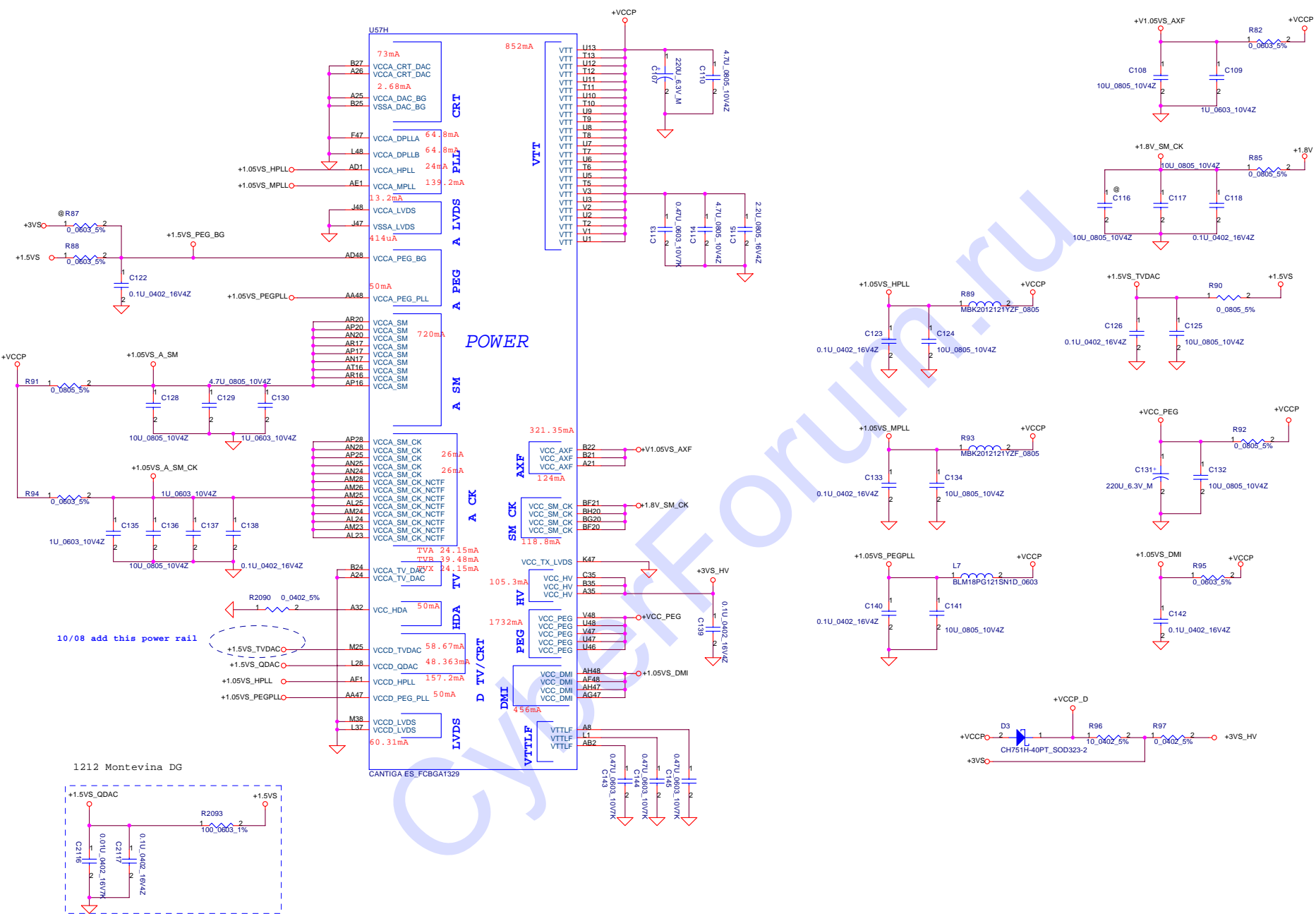
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz Selected By CPU 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chiper suite with no confidentiality 1=(TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15>0, 14>1 1 = Normal Operation,Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu. *



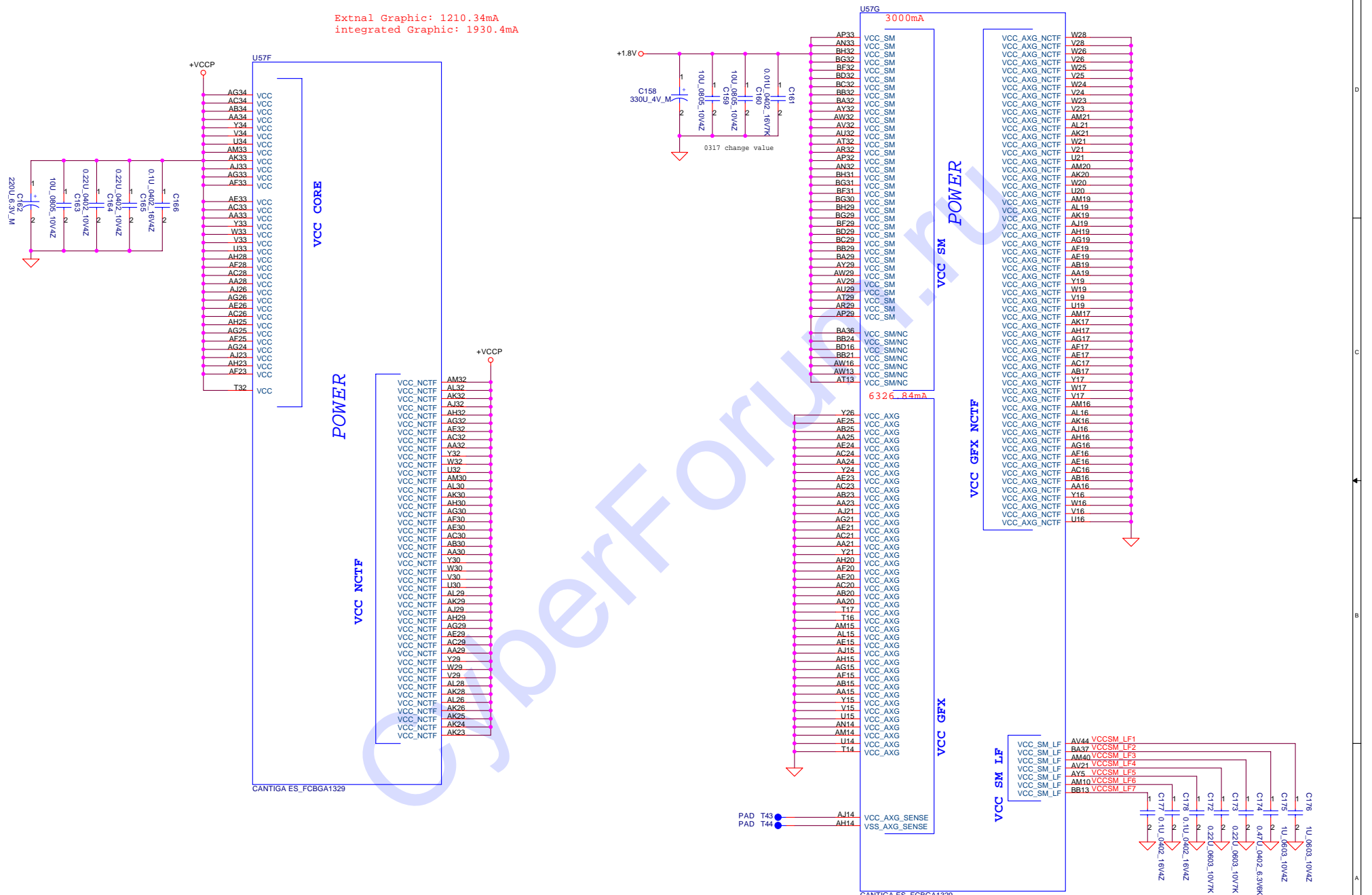
MV1 No-stuff R59,R67,R65,R77,R66

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Issued Date	2006/02/13	Deciphered Date	2006/03/10	Cantiga(3/6)-VGA/LVDS/TV	
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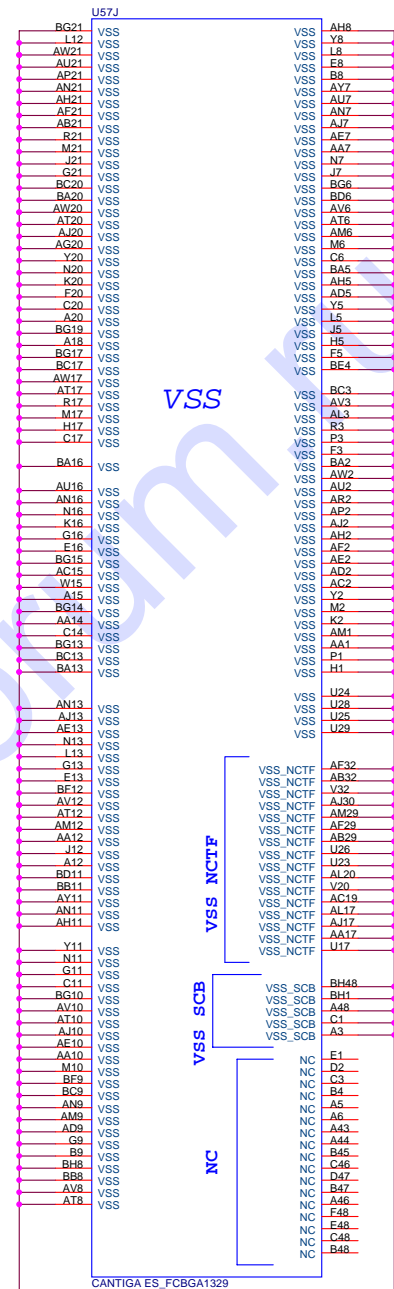
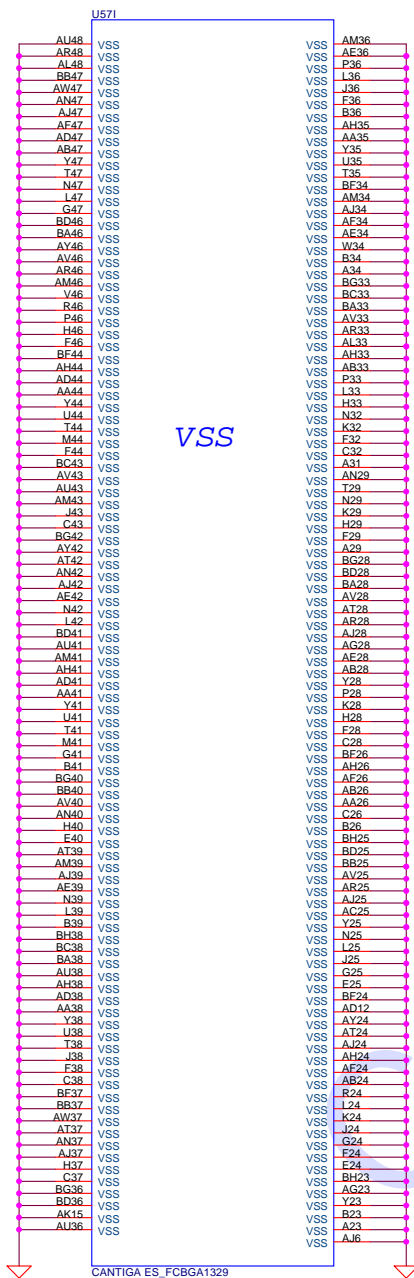
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Extenal Graphic: 1210.34mA
 integrated Graphic: 1930.4mA



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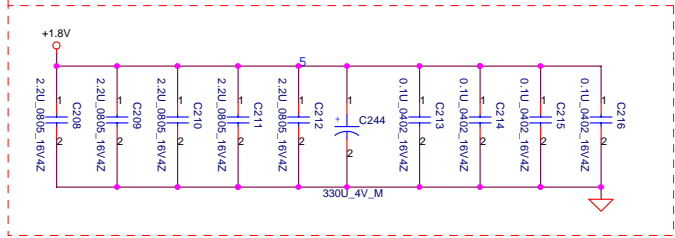
Title		Size	Document Number	Rev
Compal Electronics, Inc.		Custom	LA-4082P Vader Discrete	0.2
Cantiga(5/6)-PWR/GND		Date:	Wednesday, April 30, 2008	Sheet 11 of 61



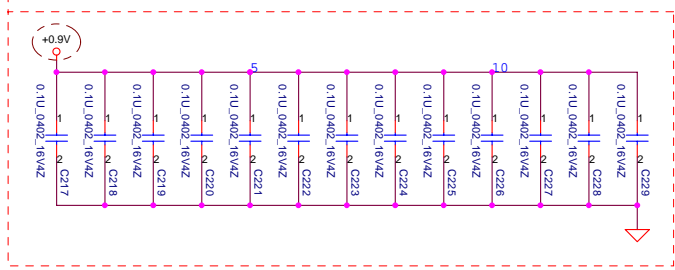
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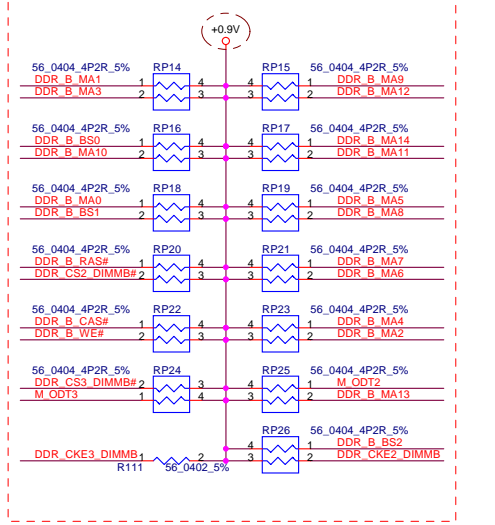
Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor closely JP3, all trace length Max=1.5"

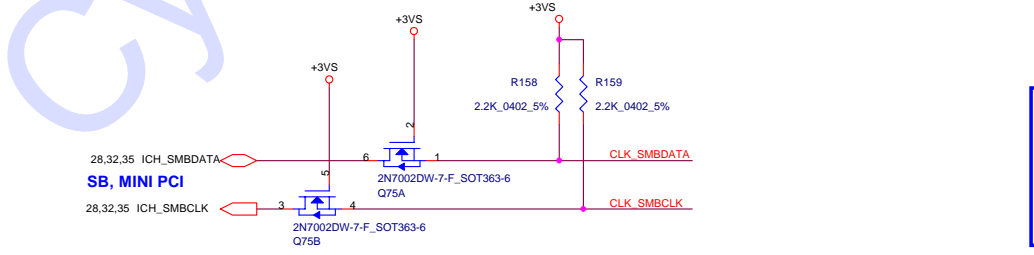
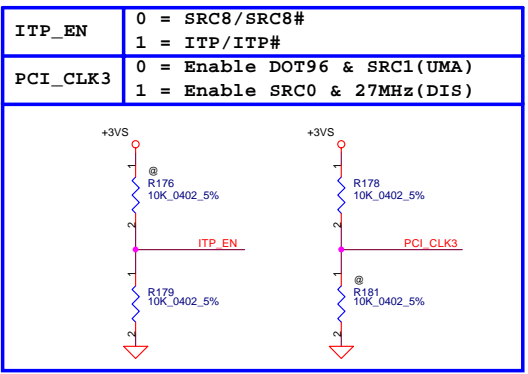
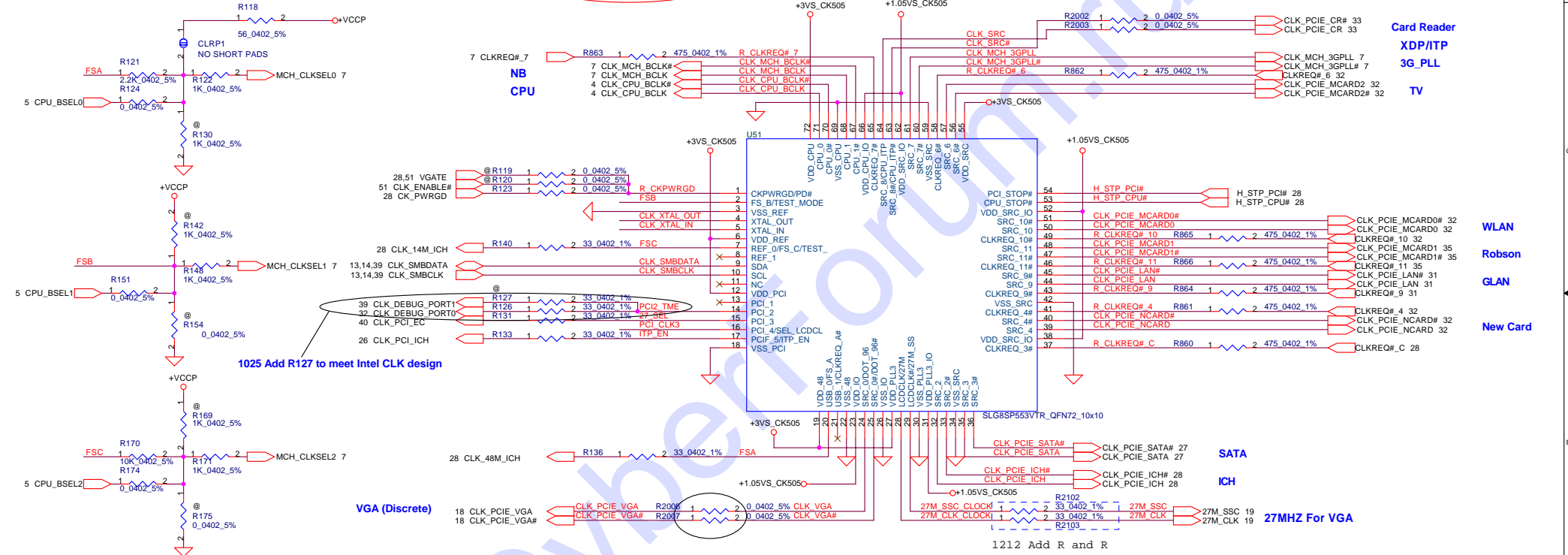
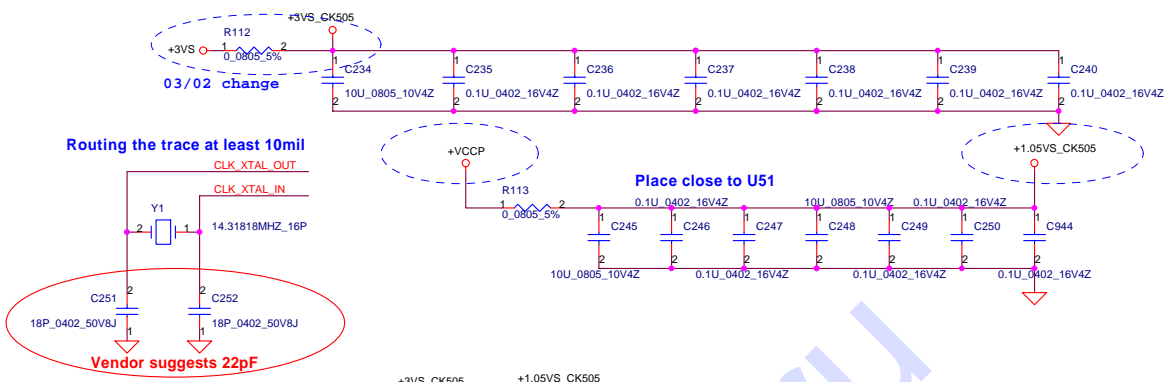


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Title		Compal Electronics, Inc.	
		DDRII-SODIMM SLOT2	
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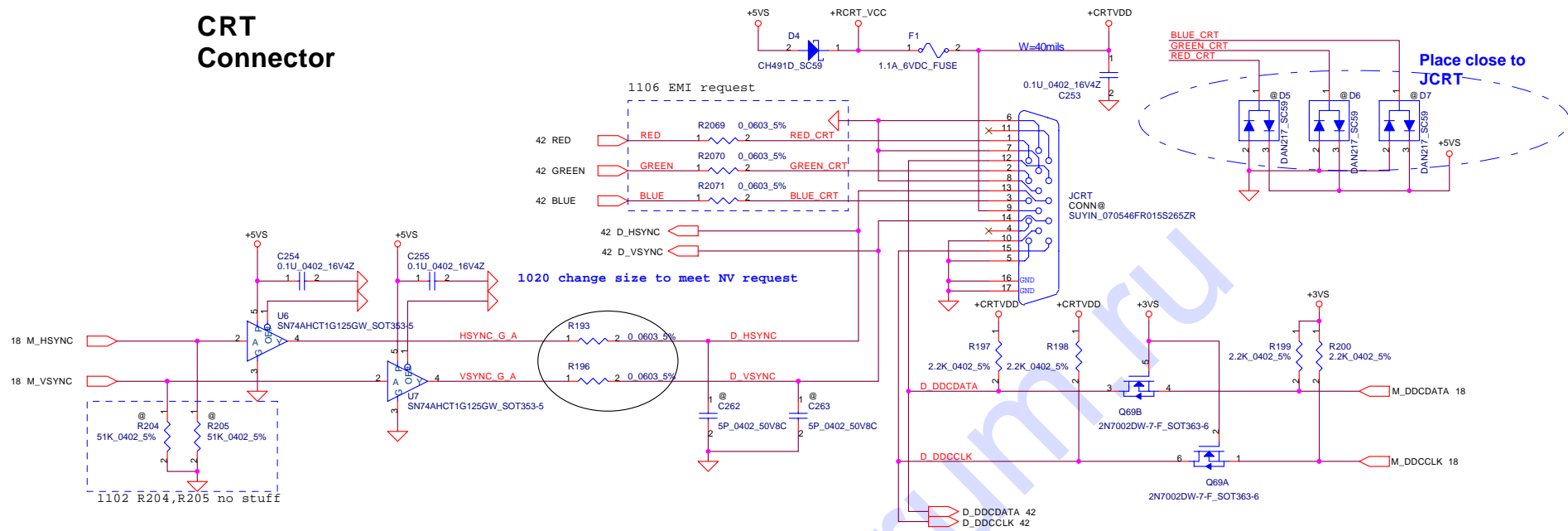
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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB	
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz	
0	0	0	266	100	33.3	14.318	96.0	48.0	
0	0	1	133	100	33.3	14.318	96.0	48.0	
0	1	0	200	100	33.3	14.318	96.0	48.0	
0	1	1	166	100	33.3	14.318	96.0	48.0	
1	0	0	333	100	33.3	14.318	96.0	48.0	
1	0	1	100	100	33.3	14.318	96.0	48.0	
1	1	0	400	100	33.3	14.318	96.0	48.0	
1	1	1	Reserved						



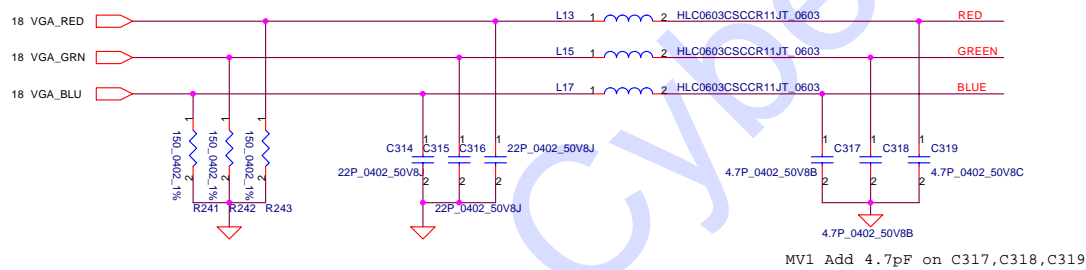
@ C232	5P_0402_50V8C	2	1	CLK_48M_ICH
@ C233	4.7P_0402_50V8C	2	1	CLK_14M_ICH
@ C241	4.7P_0402_50V8C	2	1	CLK_PCI_ICH
@ C242	4.7P_0402_50V8C	2	1	CLK_PCI_EC
@ C243	5P_0402_50V8C	2	1	CLK_DEBUG_PORT0

CRT Connector



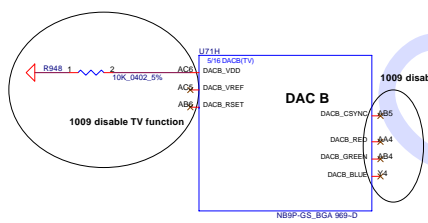
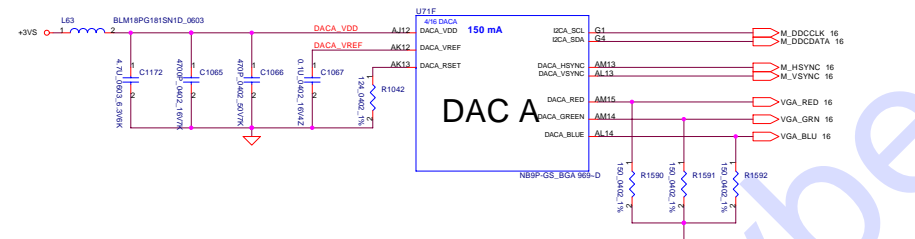
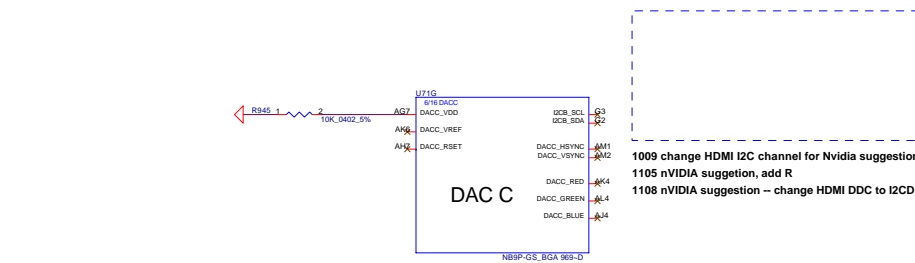
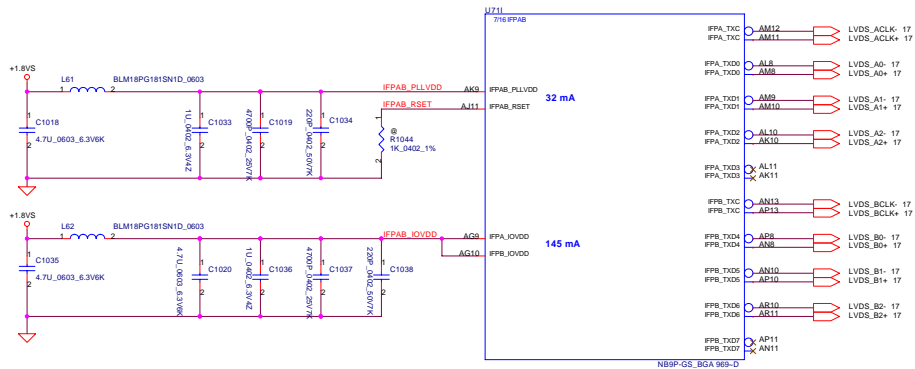
CRT Termination/EMI Filter

Note: CRT / TV-out should route to JP30 first then to the JP1 & JP2 on system side.

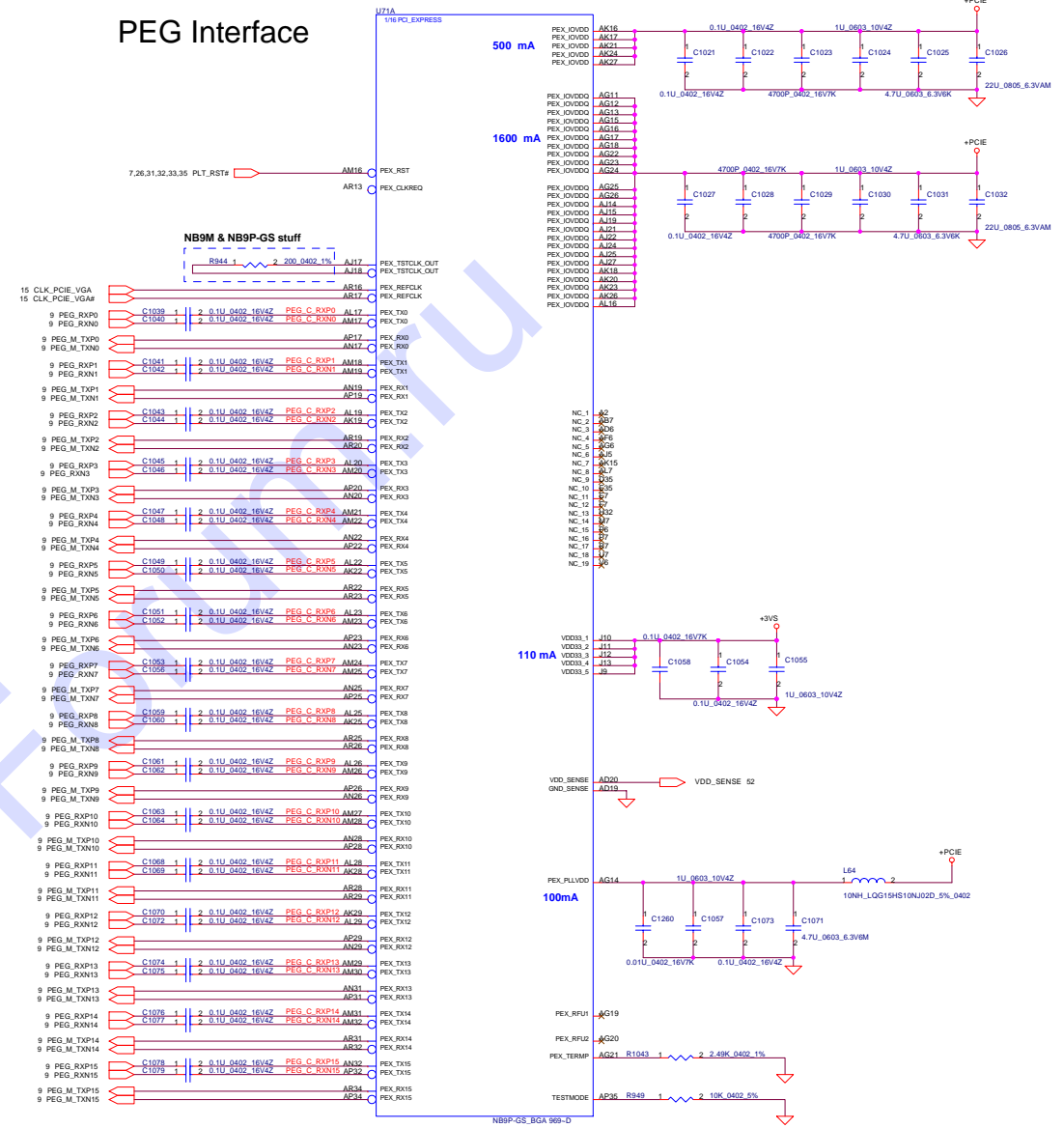


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				LA-4082P Vader Discrete		0.2
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LVDS & DAC Interface



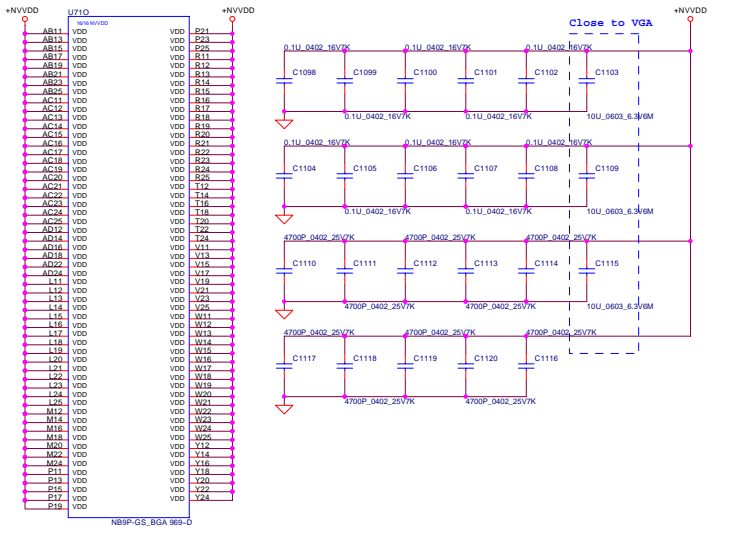
PEG Interface



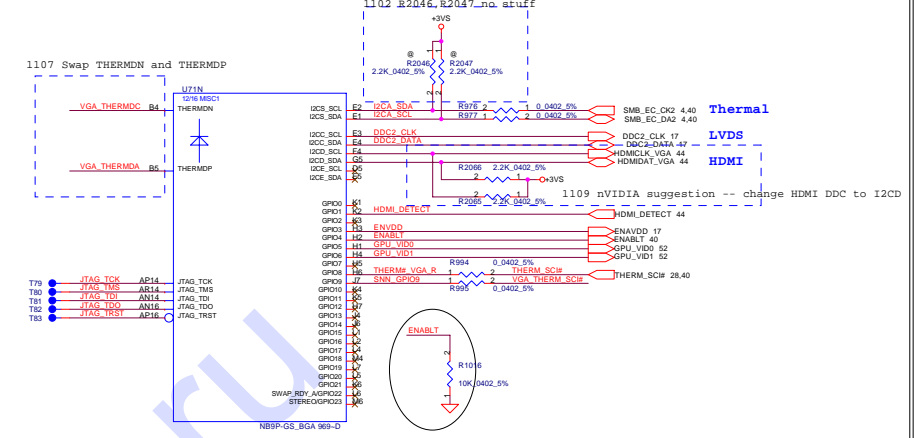
Security Classification	Compal Secret Data		Title
Issued Date	2006/02/13	Deciphered Date	2006/03/10
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Size	Document Number	Rev	0.2
Customer	LA-4082P Vader Discrete	Date	Tuesday, Aug 29, 2006
		Sheet	18 of 61

Compal Electronics, Inc.
PEG & LVDS & DAC

VGA Core power

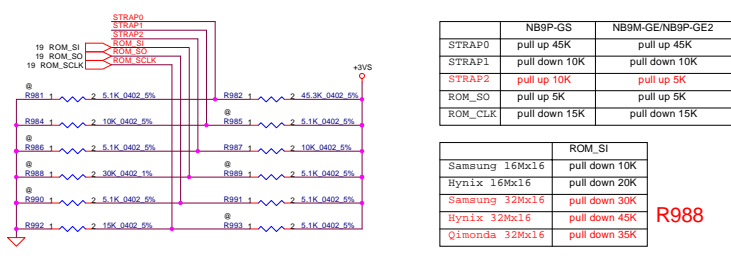


GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	Primary DVI Hot-plug
GPIO1	IN	N/A	2nd DVI Hot-plug
GPIO2	OUT	H	Panel Back-Light PWM
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light Enable
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	OUT	N/A	FBVDD VID0
GPIO8	IN	L	Thermal Alert
GPIO9	OUT	L	FAN PWM
GPIO10	OUT	N/A	FBVref Select
GPIO11	OUT	N/A	SLI SYNC
GPIO12	IN	N/A	AC Detect
GPIO13	OUT	L	PS Control or HDMI_CEC
GPIO14	OUT	H	PS Control



MULTI LEVEL STRAPS For NB9M-Gx (64bit)

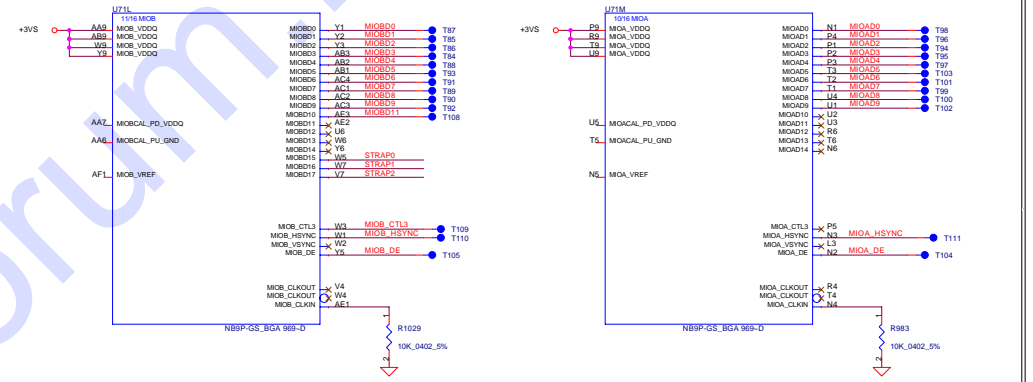
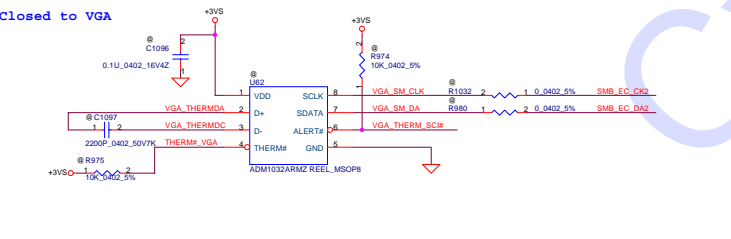
NB9P-GS and NB9P-GE2 is as same as NB9M-GE-B



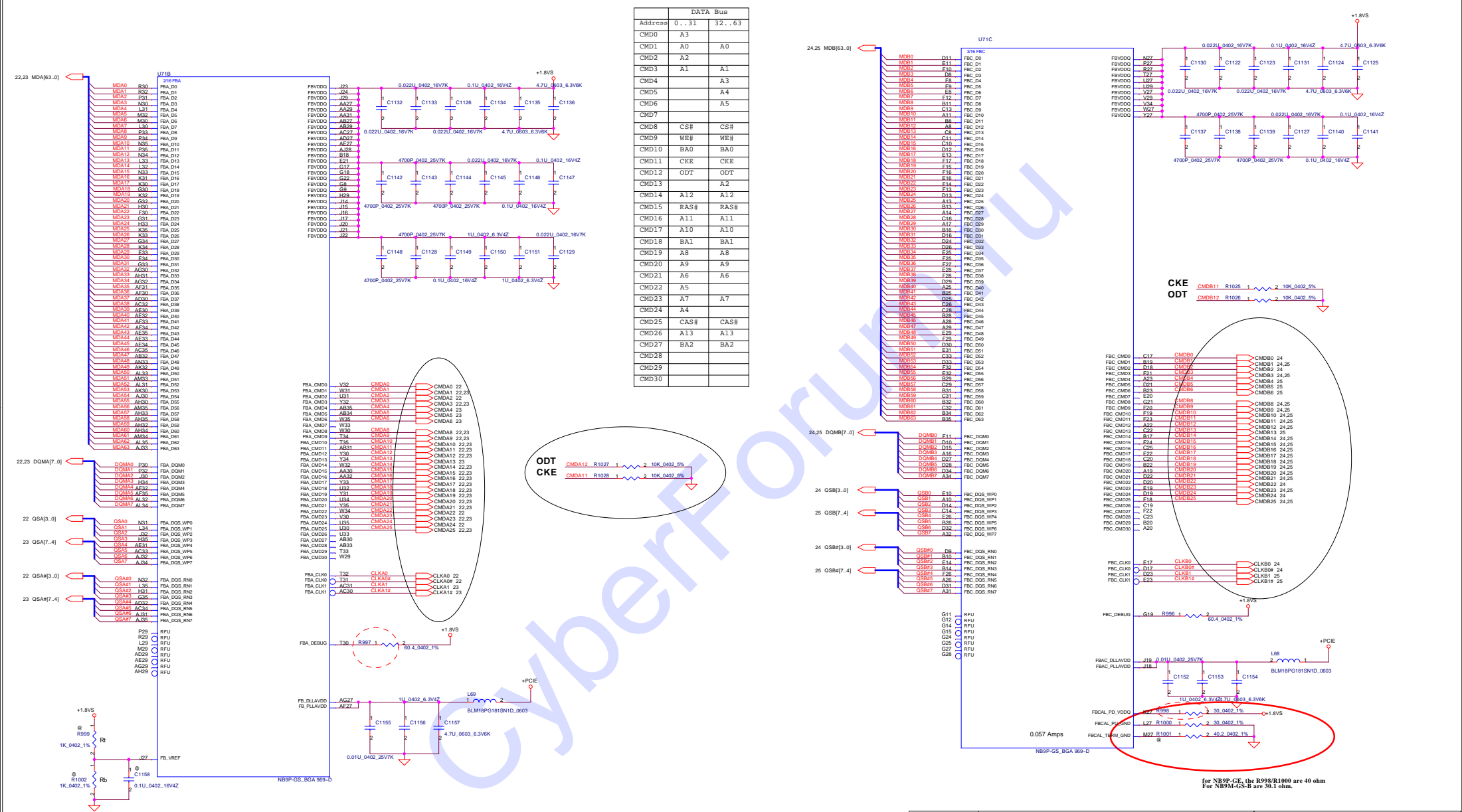
STRAP2 -- R987

R988

VGA Thermal Sensor ADM1032ARMZ



VRAM Interface



ODT CKE
 CMDA13 R1027 1 2 10K 0402 5%
 CMDA11 R1028 1 2 10K 0402 5%

For NB9P-GE, the R998/R1000 are 40 ohm
 For NB9M-GS-B are 30.1 ohm.

VREF = 0.5 * FBVDDQ
 DDR2: 1.0V = 2.0V * 1K/(1K + 1K)
 FBVREF = FBVDDQ * Rb/(Rt + Rb)

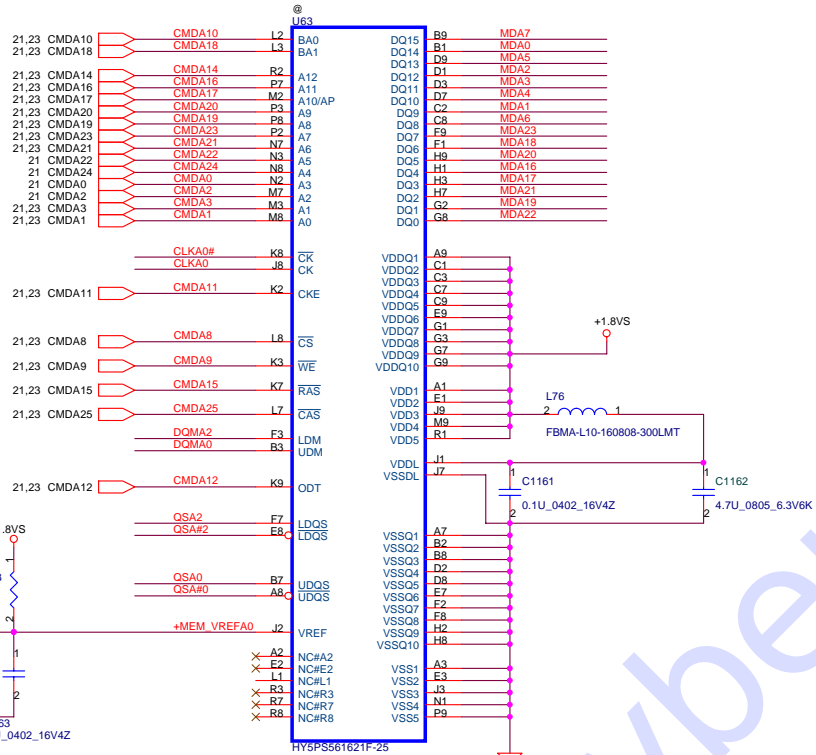
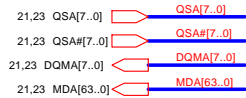
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Issued Date	2006/02/13	Deciphered Date
Issue	2006/03/10	Issue
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Size	Document Number	Rev
Customer	LA-4082P Vader Discrete	0.2
Date	Tuesday, April 29, 2008	Sheet 21 of 61

VRAM Interface

VRAM DDR2 chips (256MB & 512MB)

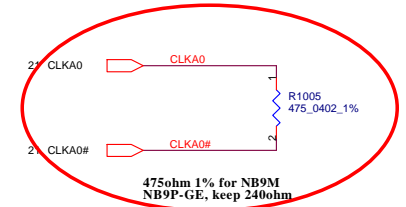
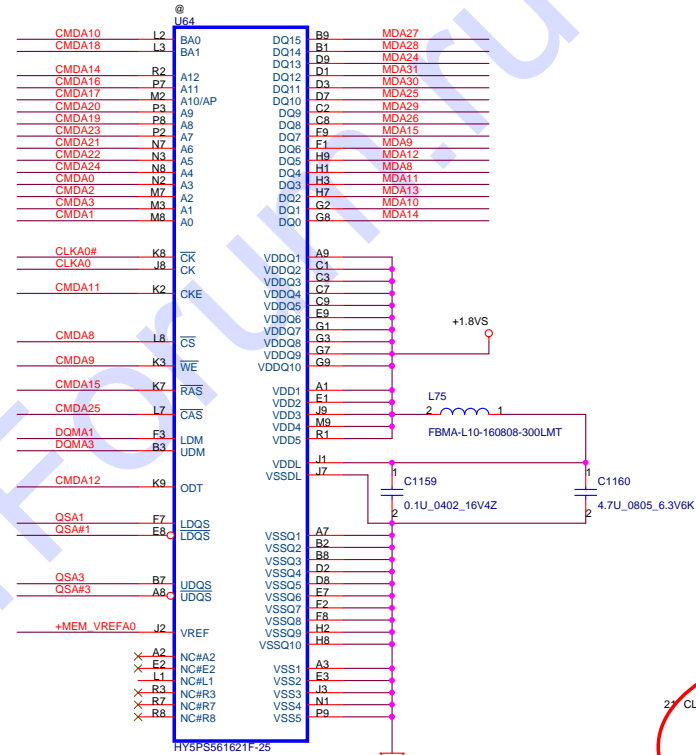
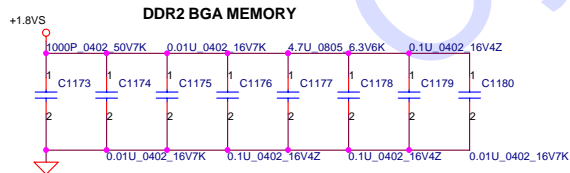
32Mx16 DDR2 400MHz *8==>512MB

32Mx16 DDR2 400MHz *4==>256MB

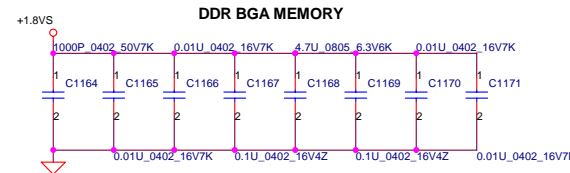


Vref= 0.5* 1.8V for NB9M, R1004=1K ohm

Vref= 0.5* 1.8V for NB9P-GS/GE2, R1004=1K ohm



475ohm 1% for NB9M NB9P-GE, keep 240ohm

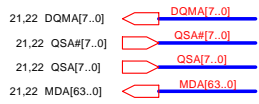


	DATA Bus	
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

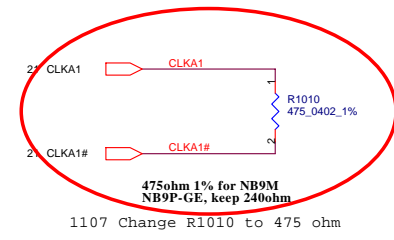
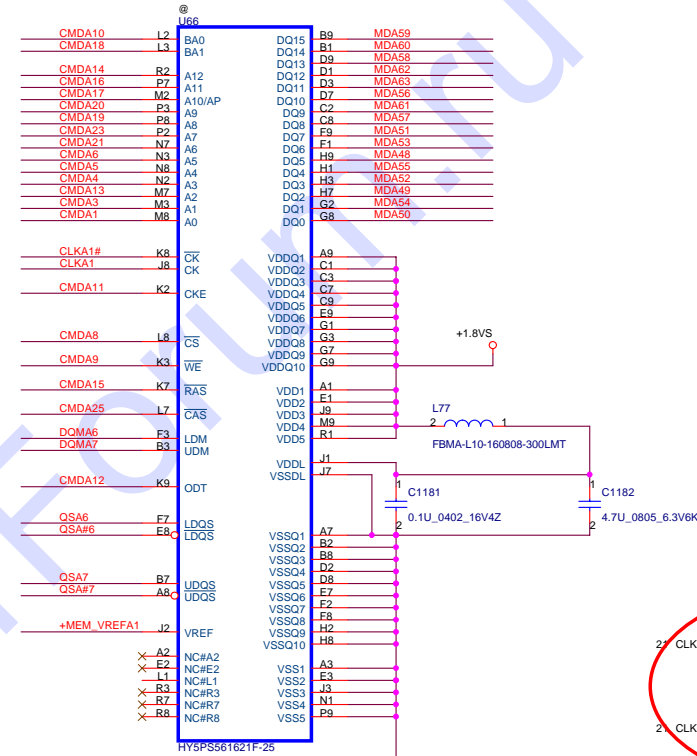
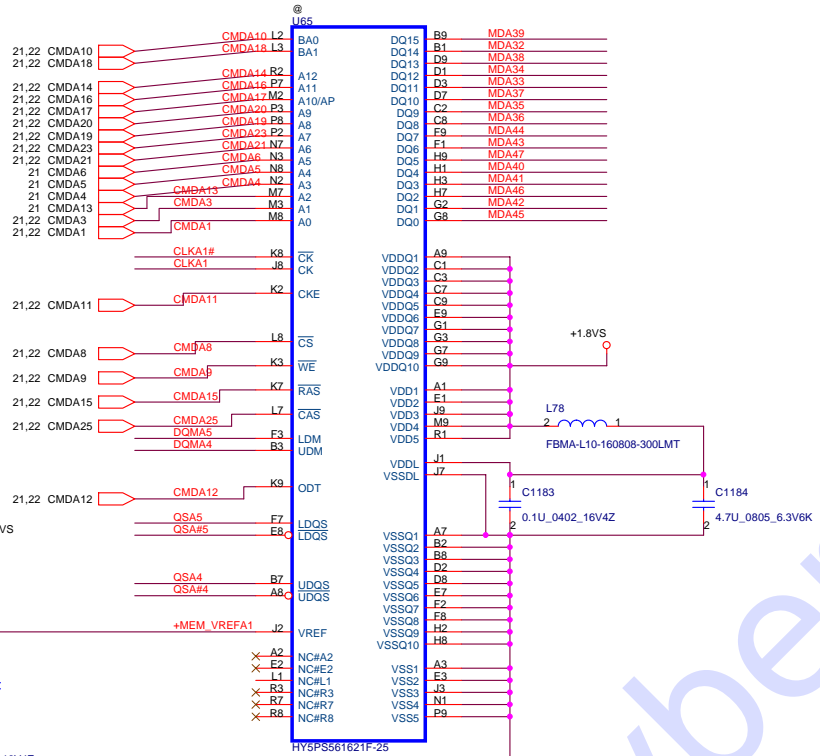
VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *8==>512MB

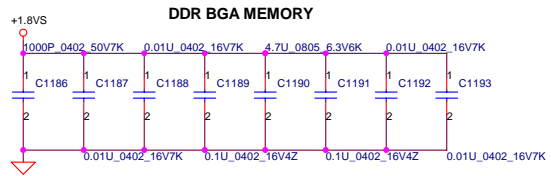
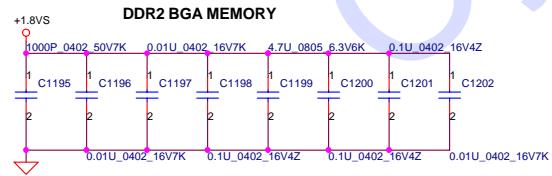
32Mx16 DDR2 400MHz *4==>256MB



Address	DATA Bus	
	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		A2
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



Vref= 0.5* 1.8V for NB9M, R1009=1K ohm
 Vref= 0.5* 1.8V for NB9P-GS/GE2, R1009=1K ohm



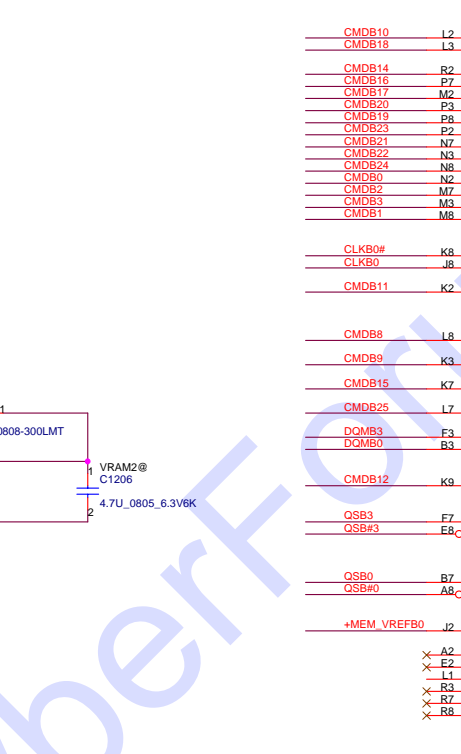
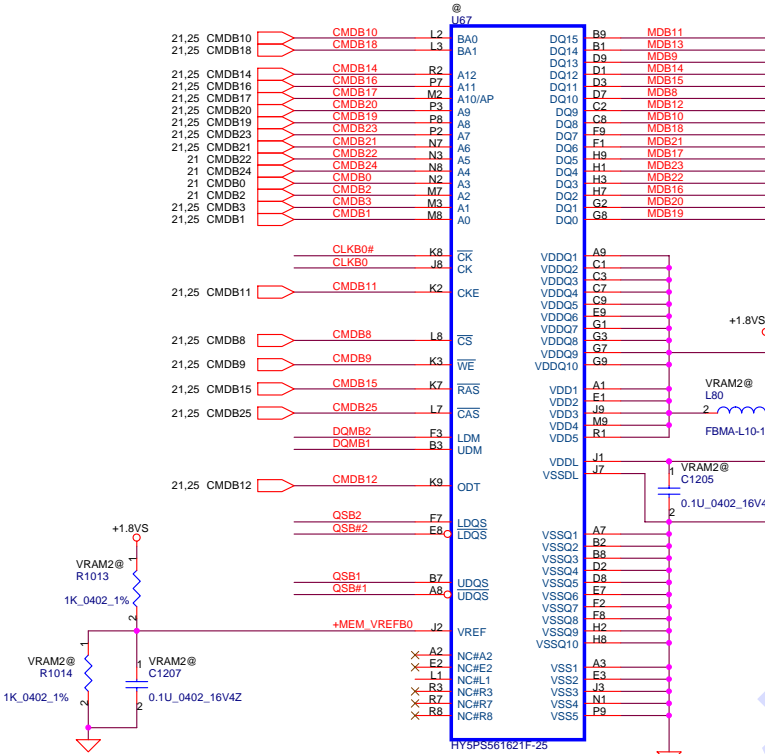
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Size	Document Number	Rev	Date: Tuesday, April 29, 2008 Sheet 23 of 61	
Customer	LA-4082P Vader Discrete	0.2		

VRAM DDR2 chips (256MB & 512MB)

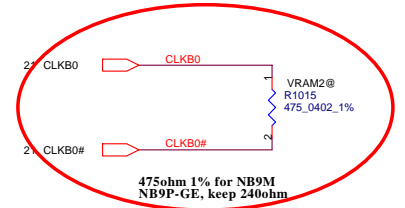
32Mx16 DDR2 400MHz *8==>512MB



		DATA Bus	
Address	0..31	32..63	
CMD0	A3		
CMD1	A0	A0	
CMD2	A2		
CMD3	A1	A1	
CMD4		A3	
CMD5		A4	
CMD6		A5	
CMD7			
CMD8	CS#	CS#	
CMD9	WE#	WE#	
CMD10	BA0	BA0	
CMD11	CKE	CKE	
CMD12	ODT	ODT	
CMD13		A2	
CMD14	A12	A12	
CMD15	RAS#	RAS#	
CMD16	A11	A11	
CMD17	A10	A10	
CMD18	BA1	BA1	
CMD19	A8	A8	
CMD20	A9	A9	
CMD21	A6	A6	
CMD22	A5		
CMD23	A7	A7	
CMD24	A4		
CMD25	CAS#	CAS#	
CMD26	A13	A13	
CMD27	BA2	BA2	
CMD28			
CMD29			
CMD30			

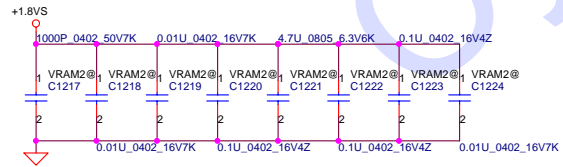


Vref= 0.5* 1.8V for NB9M, R1014=1K ohm
 Vref= 0.5* 1.8V for NB9P-GS/GE2, R1014=1K ohm

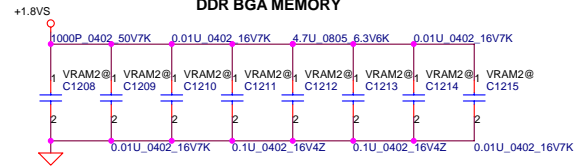


1107 Change R1015 to 475 ohm

DDR2 BGA MEMORY



DDR BGA MEMORY



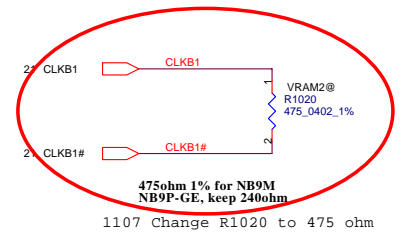
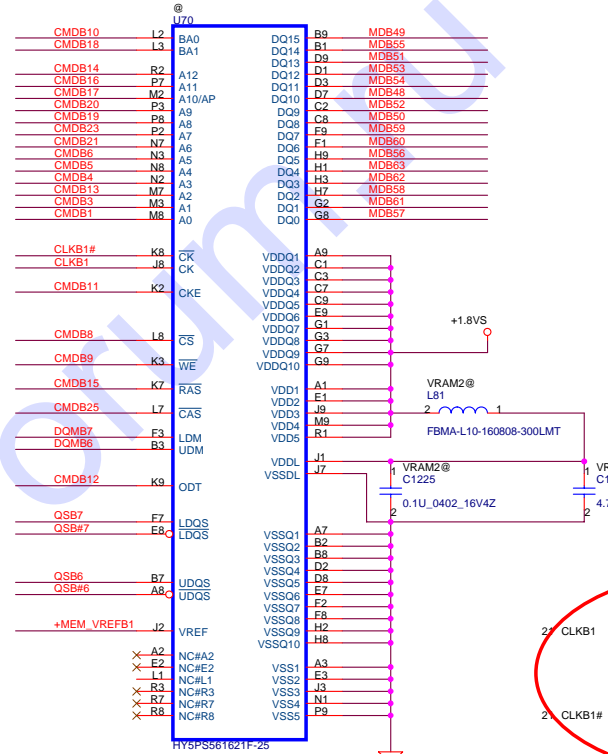
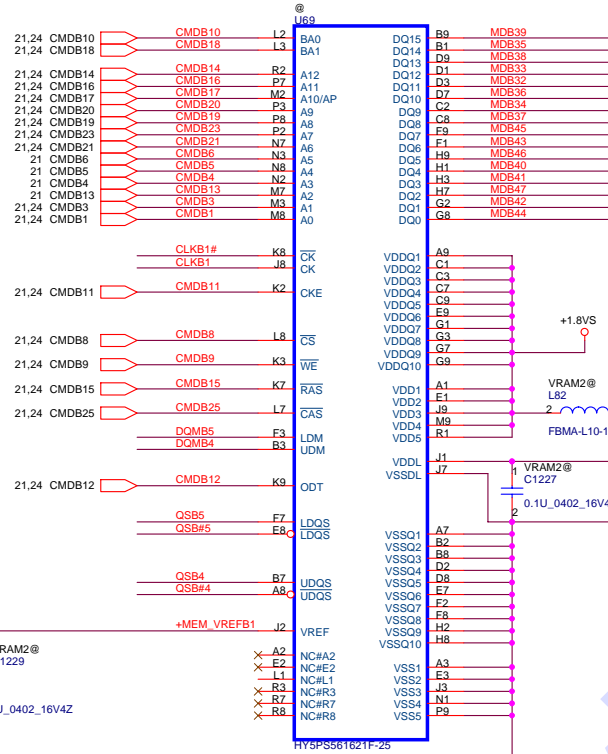
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Size	Document Number	Rev		
Customer	LA-4082P Vader Discrete	0.2		
Date	Tuesday, April 29, 2008	Sheet	24	of 61

VRAM DDR2 chips (256MB & 512MB)

32Mx16 DDR2 400MHz *8==>512MB

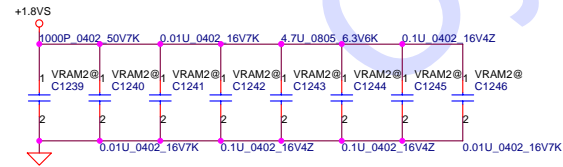


		DATA Bus	
Address	0..31	32..63	
CMD0	A3		
CMD1	A0	A0	
CMD2	A2		
CMD3	A1	A1	
CMD4		A3	
CMD5		A4	
CMD6		A5	
CMD7			
CMD8	CS#	CS#	
CMD9	WE#	WE#	
CMD10	BA0	BA0	
CMD11	CKE	CKE	
CMD12	ODT	ODT	
CMD13		A2	
CMD14	A12	A12	
CMD15	RAS#	RAS#	
CMD16	A11	A11	
CMD17	A10	A10	
CMD18	BA1	BA1	
CMD19	A8	A8	
CMD20	A9	A9	
CMD21	A6	A6	
CMD22	A5		
CMD23	A7	A7	
CMD24	A4		
CMD25	CAS#	CAS#	
CMD26	A13	A13	
CMD27	BA2	BA2	
CMD28			
CMD29			
CMD30			

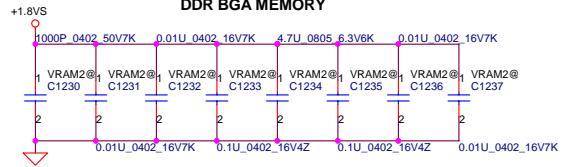


Vref= 0.5* 1.8V for NB9M, R1019=1K ohm
 Vref= 0.5* 1.8V for NB9P-GS/GE2, R1019=1K ohm

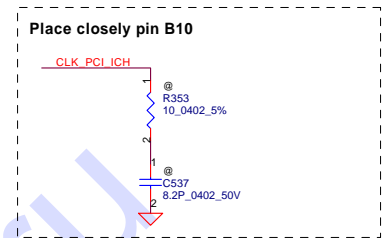
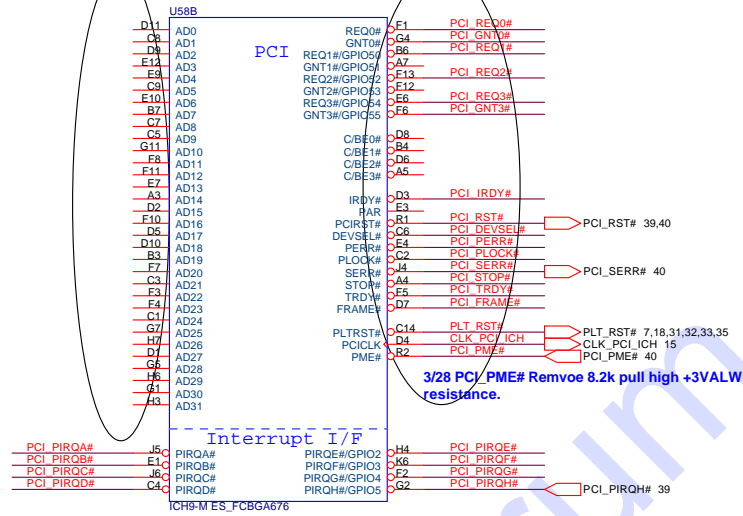
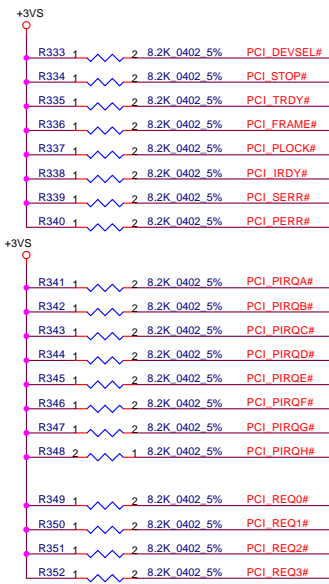
DDR2 BGA MEMORY



DDR BGA MEMORY



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Size	Document Number	Rev			
Custom	LA-4082P Vader Discrete	0.2			
Date:	Tuesday, April 29, 2008	Sheet	25	of	61



3/28 PCI_PME# Remove 8.2k pull high +3VALW resistance.

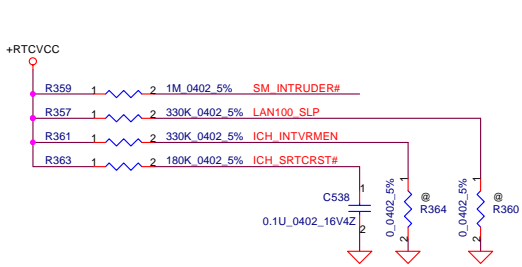
Interrupt I/F

A16 swap override Strap

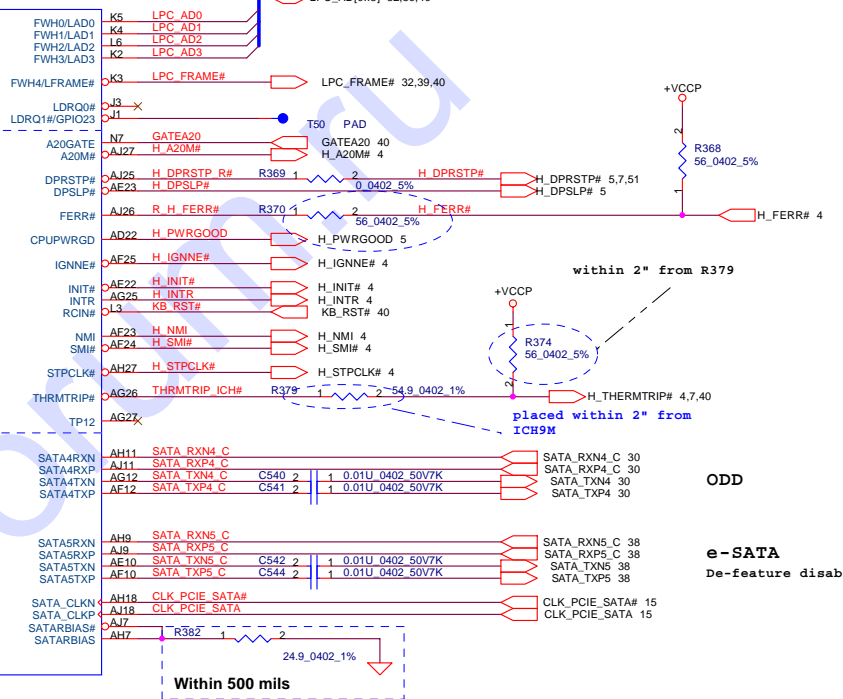
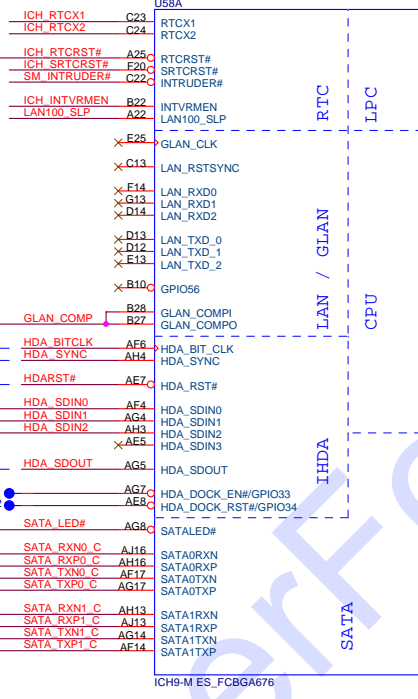
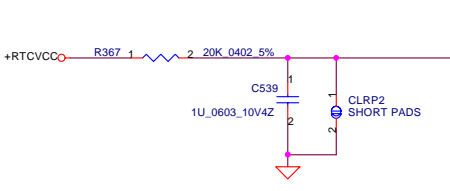
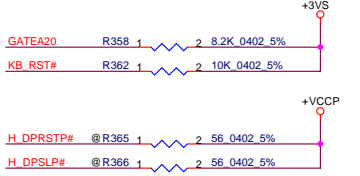
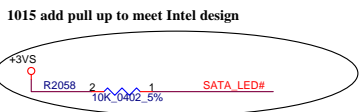
PCI_GNT3#	Low= A16 swap override Enble
	High= Default *

Boot BIOS Strap

PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

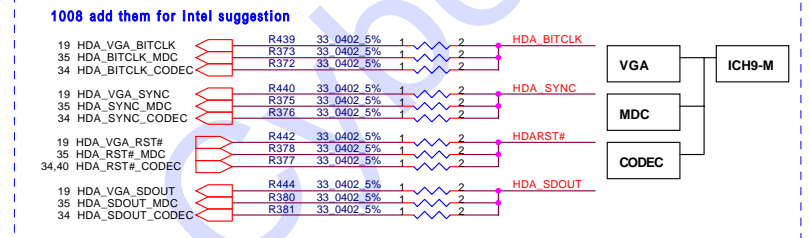
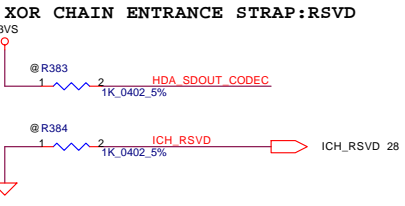


ICH9M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)



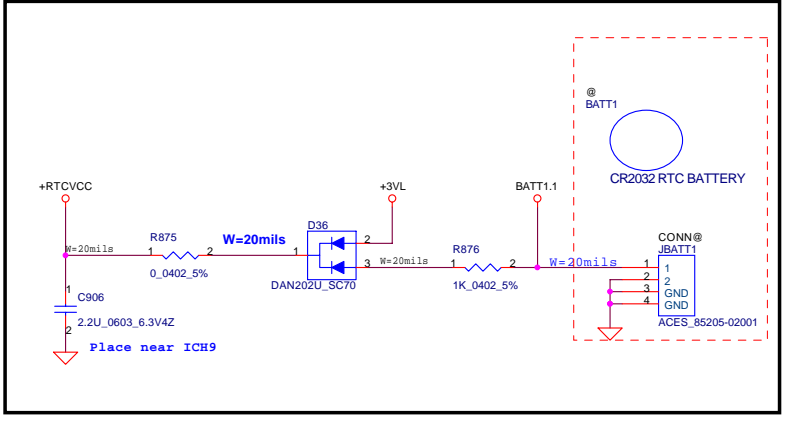
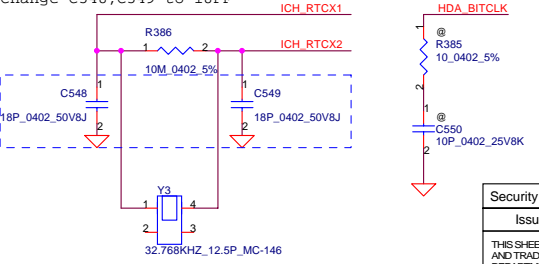
P- HDD
S- HDD
1212 Swap SATA1 and SATA4

ODD
e-SATA
De-feature disable



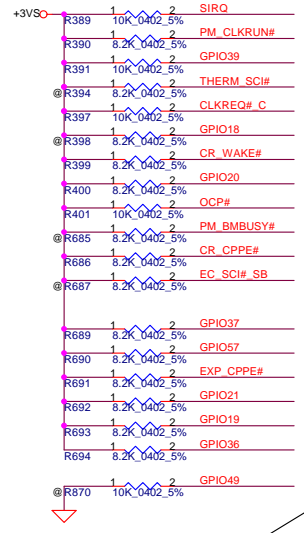
0125 Change C548, C549 to 18PF

ICH_RSVD	HDA_SDOUT_CODEC	
0	0	
0	1	
1	0	
1	1	

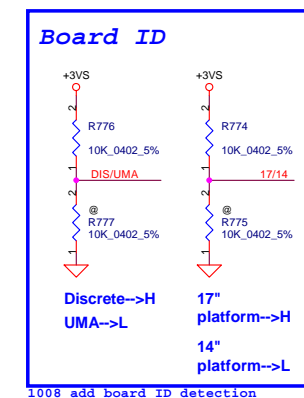
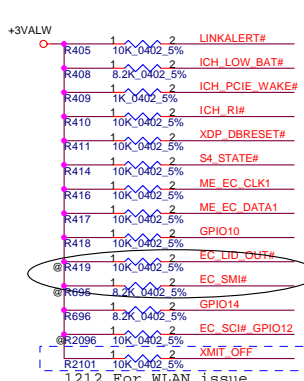


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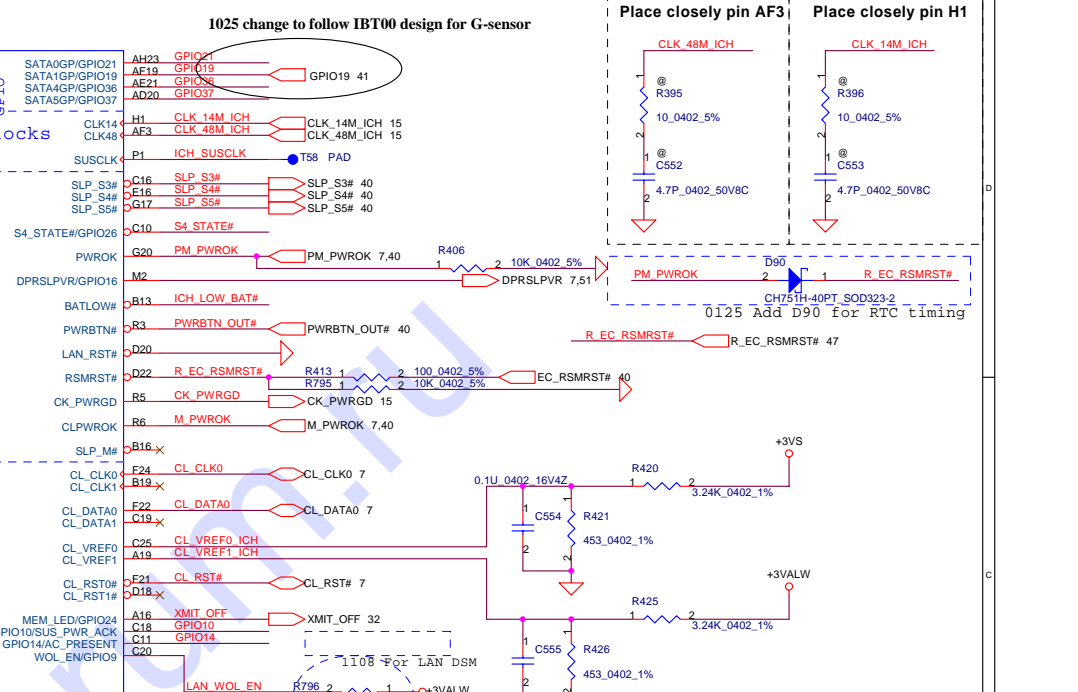
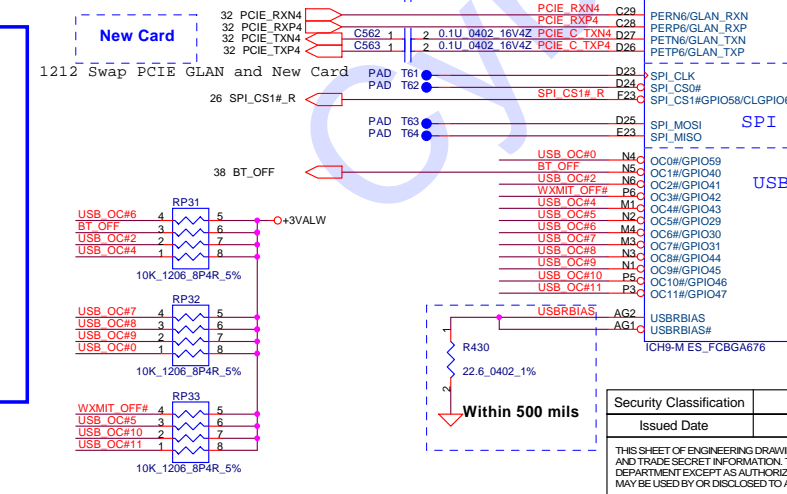
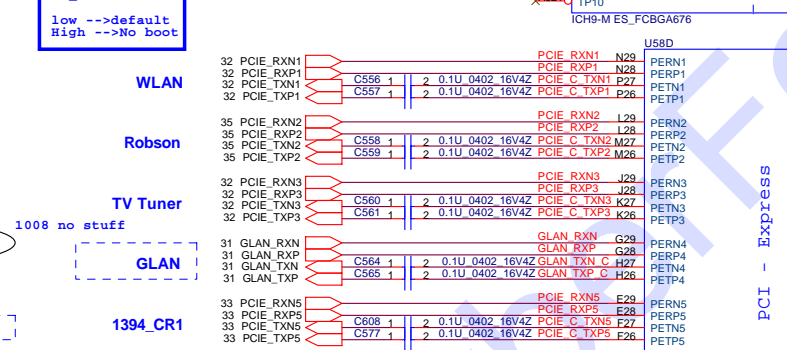
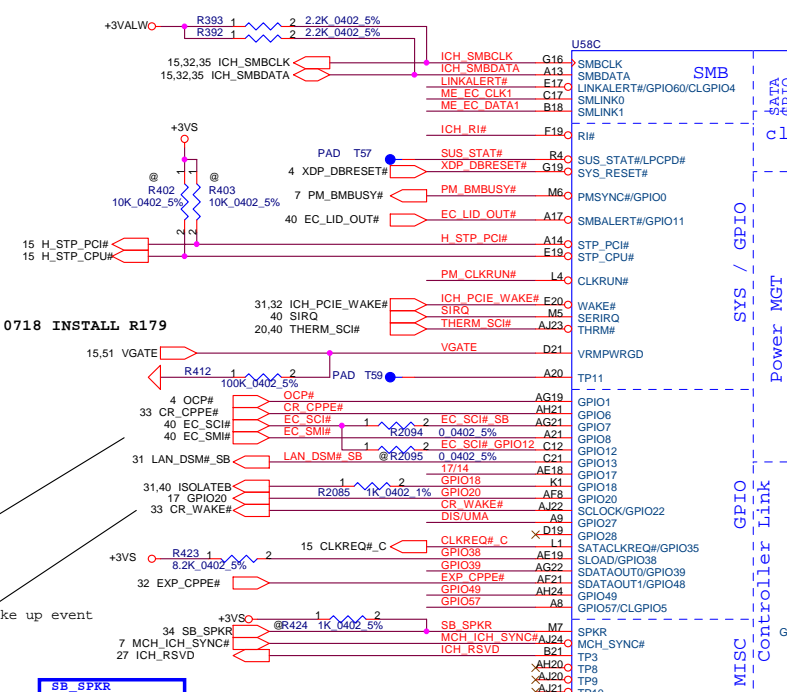
Title		Compal Electronics, Inc.	
Size		Document Number	
Custom		LA-4082P Vader Discrete	
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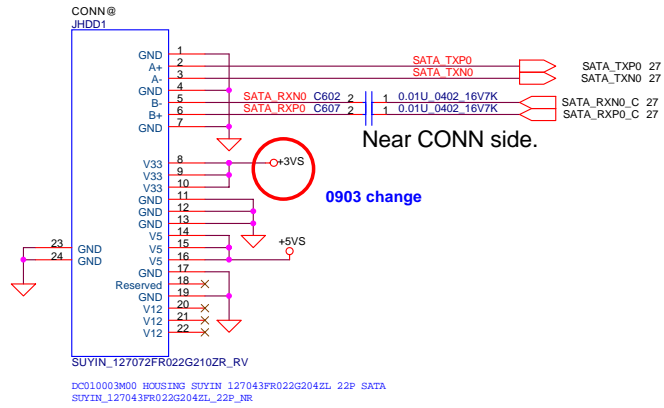
1102 Add test point
1212 Add R2095 for EC_SCI#
1108 For LAN DSM
1109 Add GPIO22 for card reader wake up event



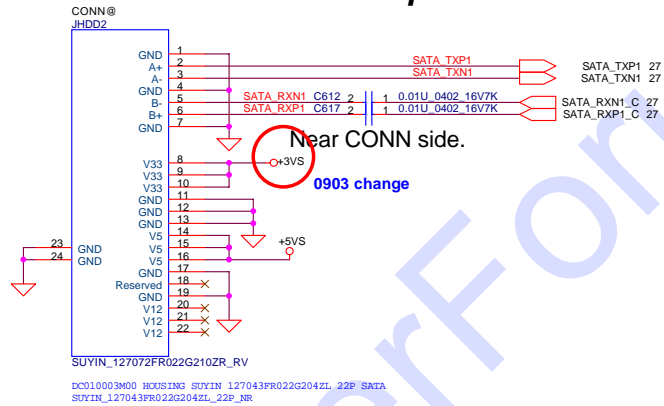
1008 add board ID detection



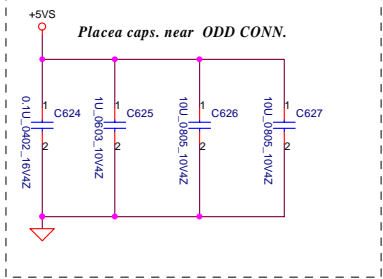
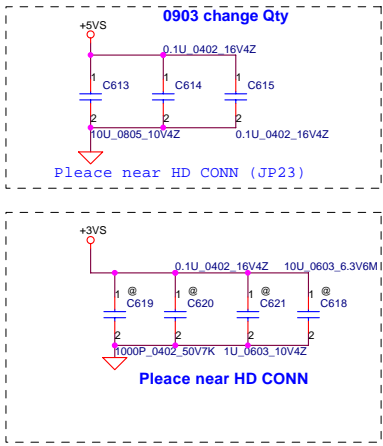
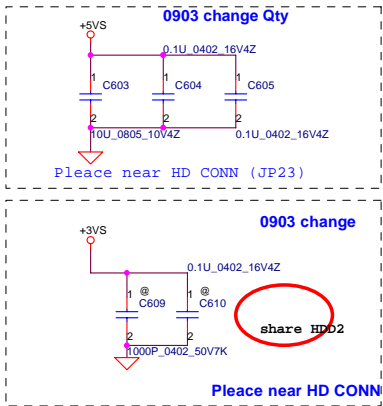
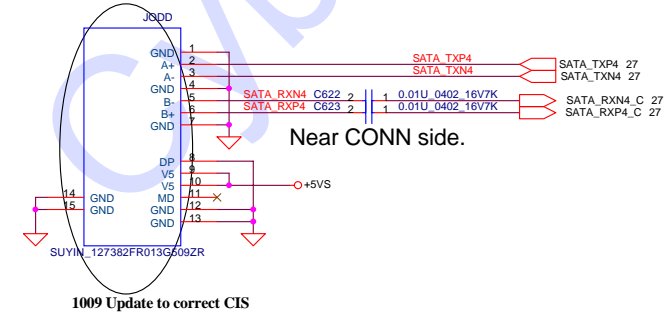
HDD Connector



2nd HDD Connector-option

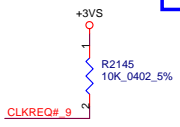
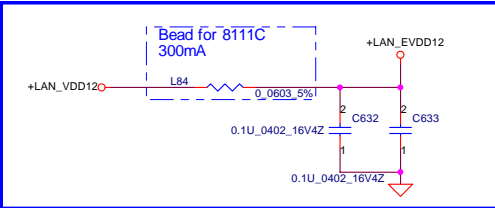
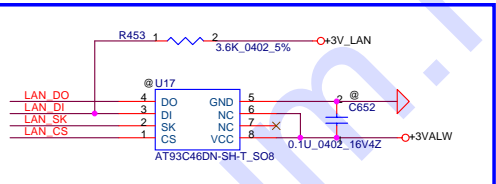
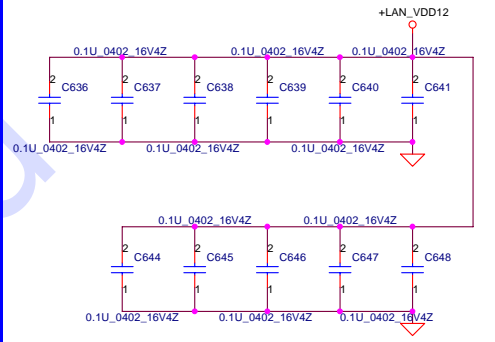
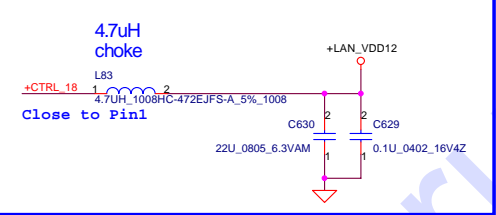
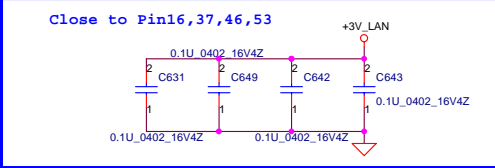
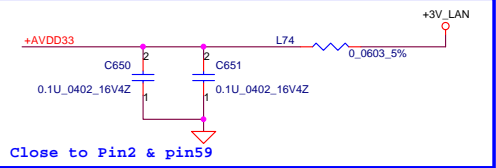
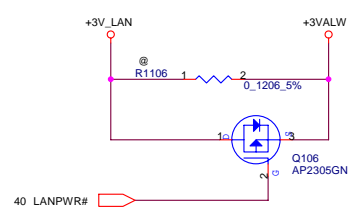


CD-ROM Connector

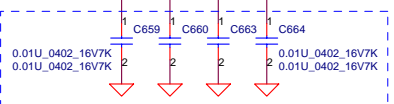
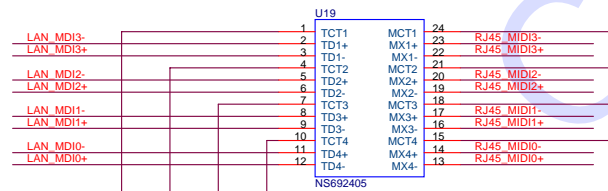
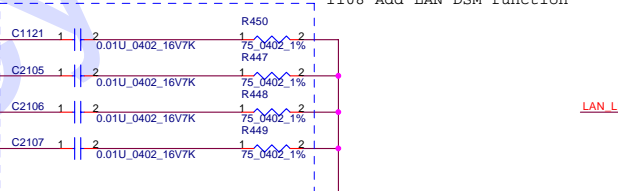
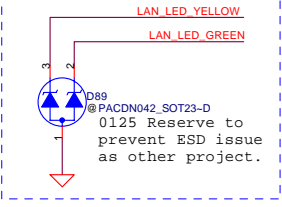
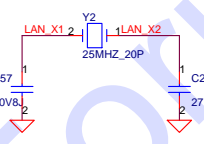
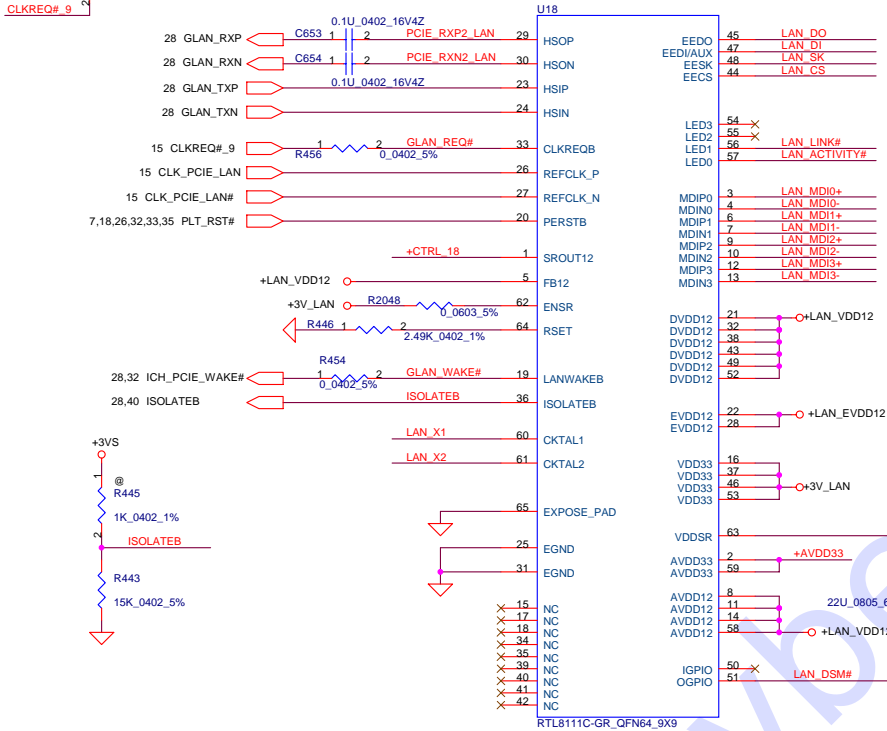


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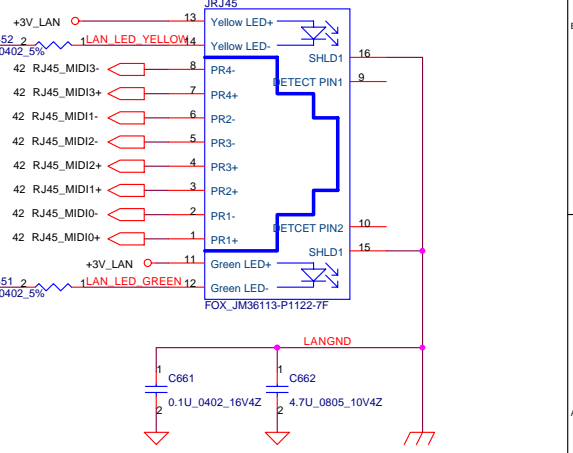
1025 add to meet HP request



Place Close to Chip



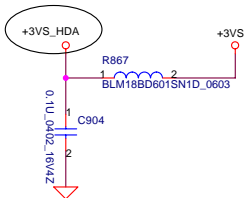
LAN Conn.



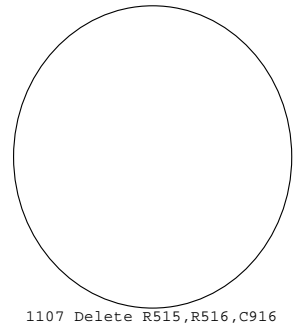
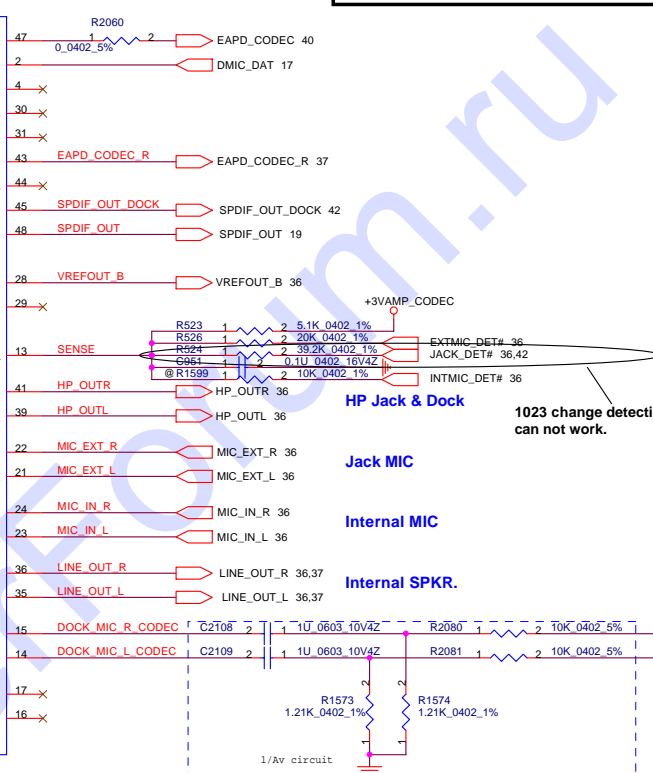
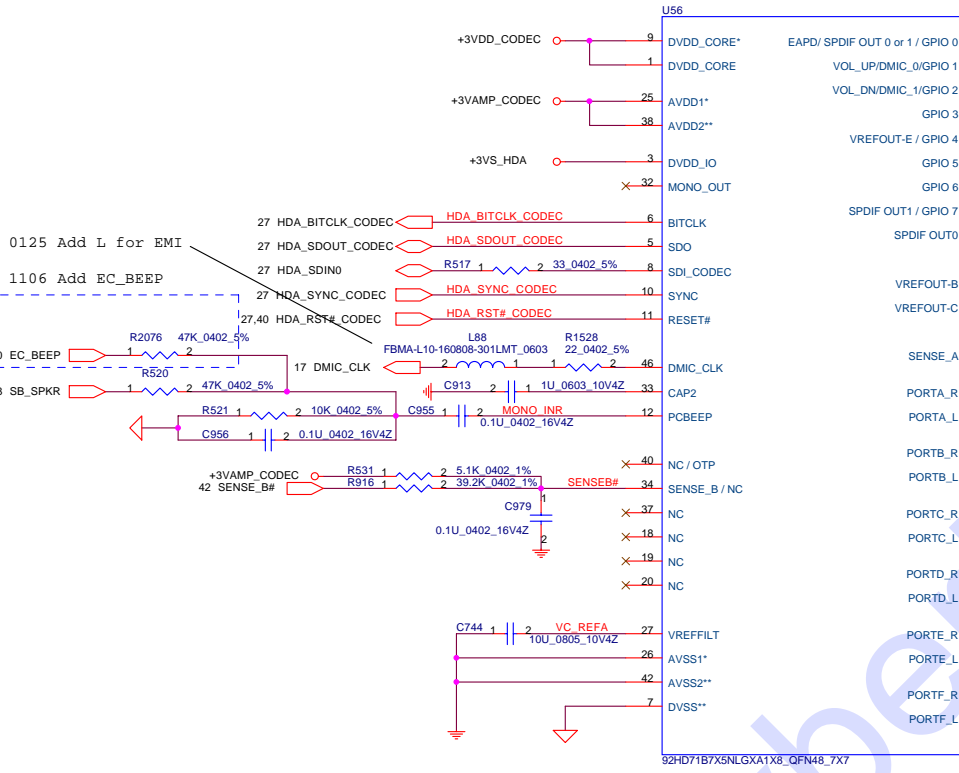
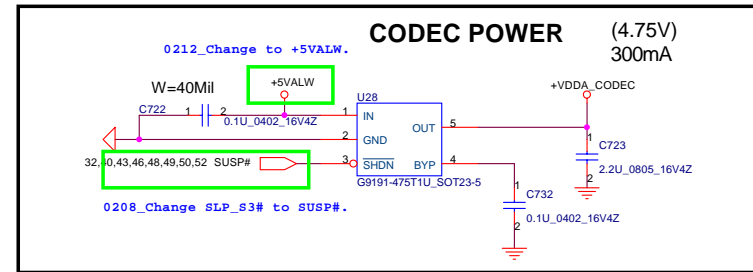
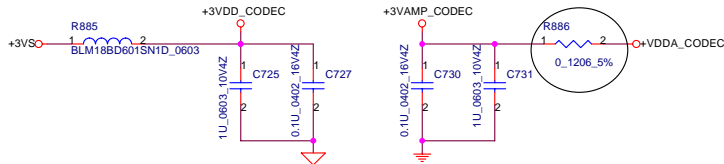
Place these components coiled to LAN blue

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1008 Change to +3V



1019 Change Size to 1206 for IDT request



0125 Add L for EMI

1106 Add EC_BEEP

28 SB_SPKR

40 EC_BEEP

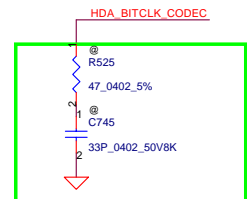
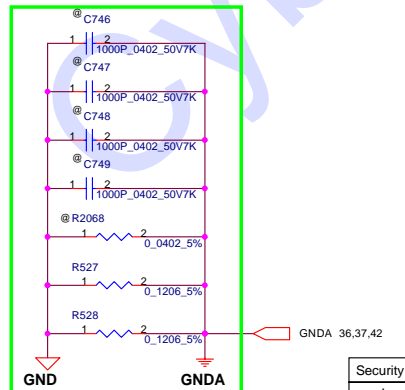
42 SENSE_B#

1106 Change C746,C747,C748,C749 to 1000PF

1023 change detection circuit to solve Speaker can not work.

1107 HP request

SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K



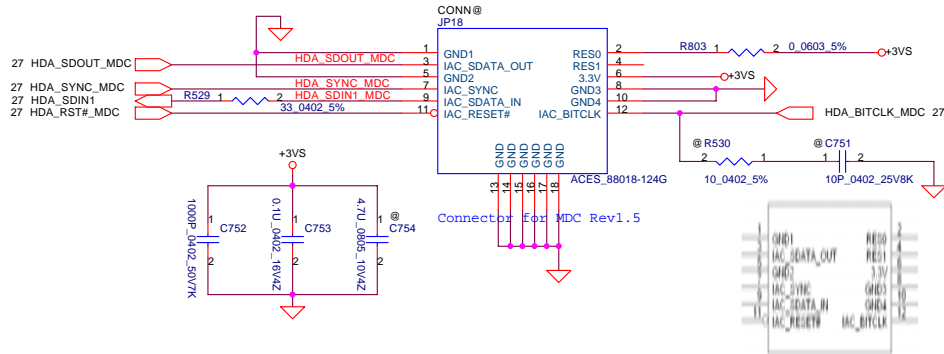
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Issued Date	2006/02/13	Deciphered Date
		2006/03/10

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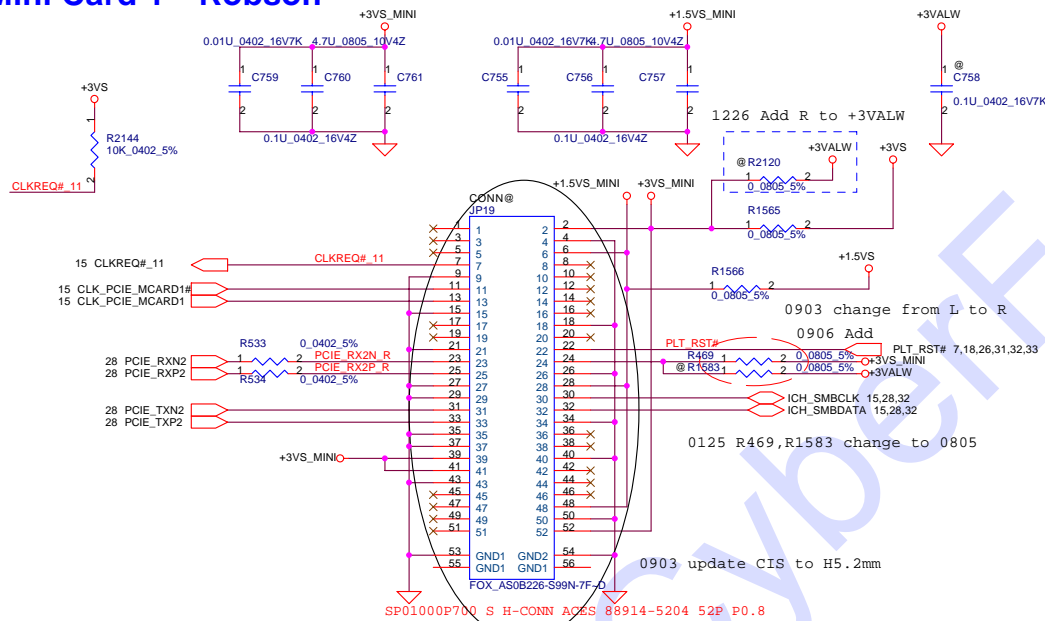
Compal Electronics, Inc.		
Title		
Codec IDT9271B7		
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MDC 1.5 Conn.

Change type 4/25



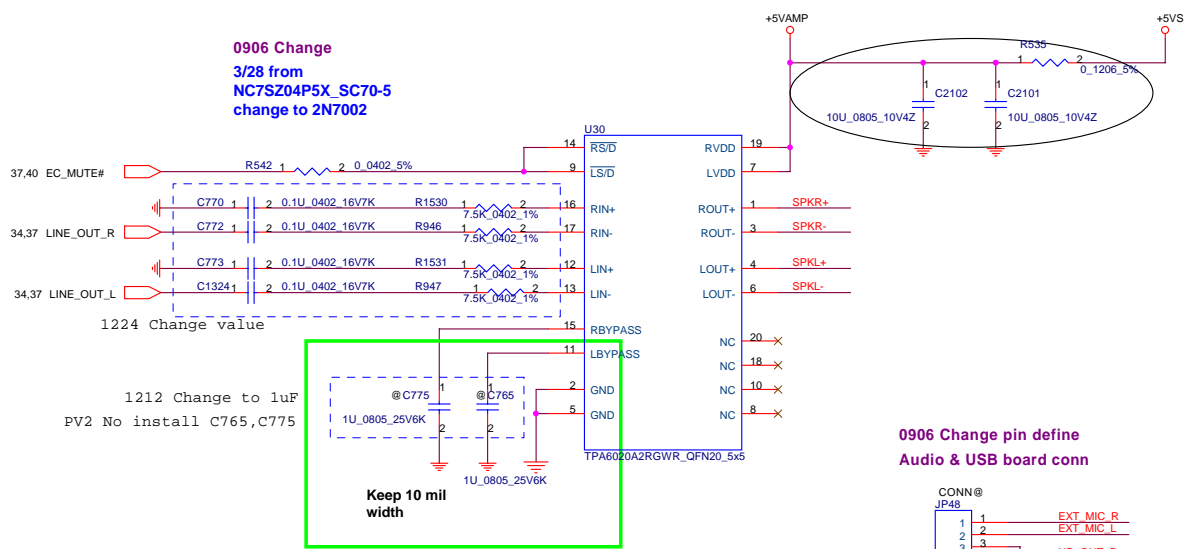
Mini Card 1---Robson



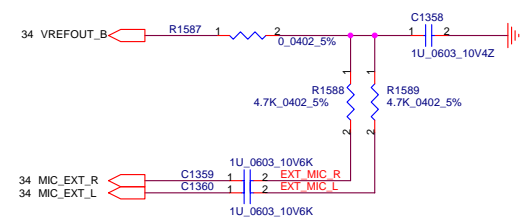
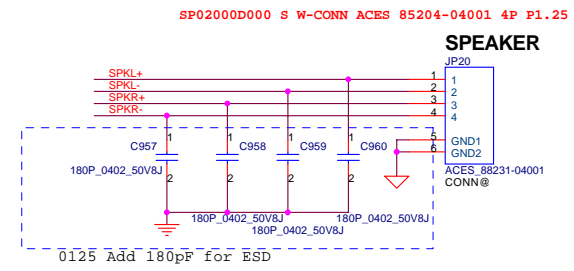
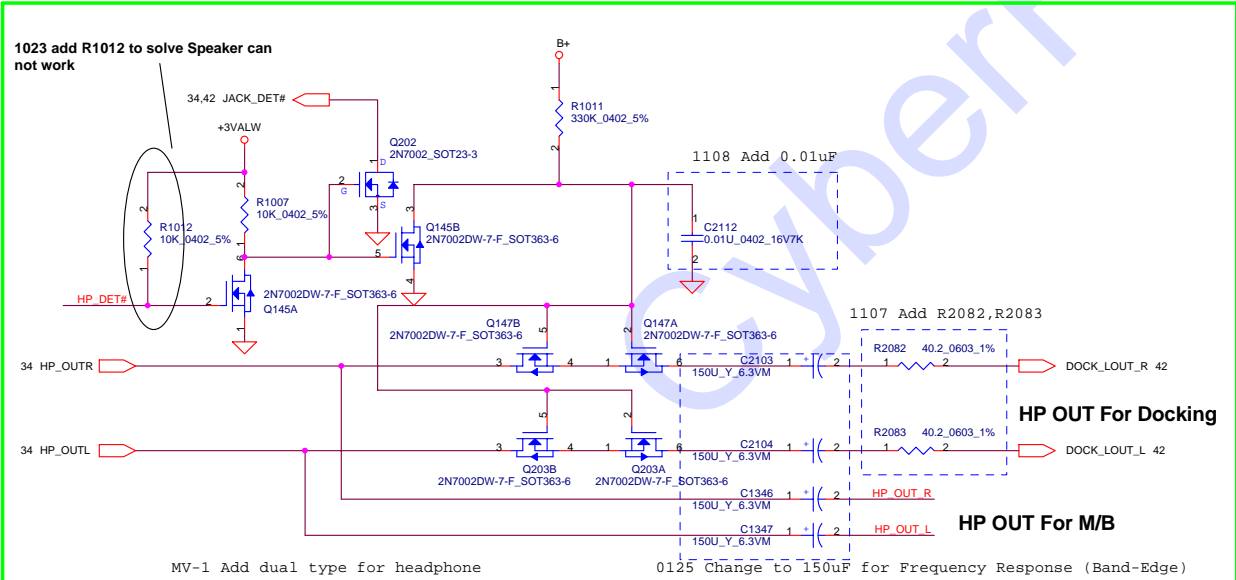
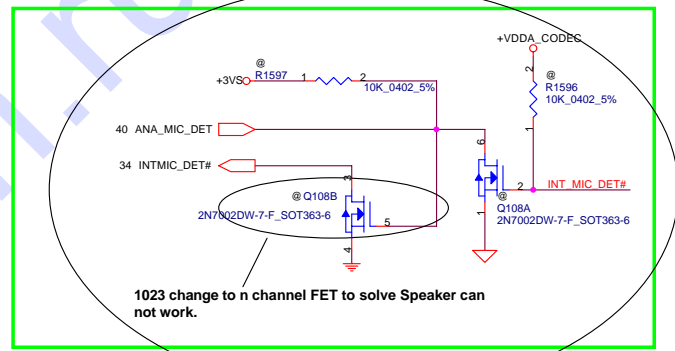
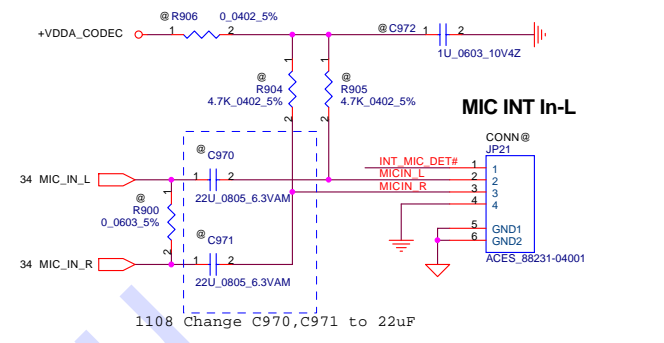
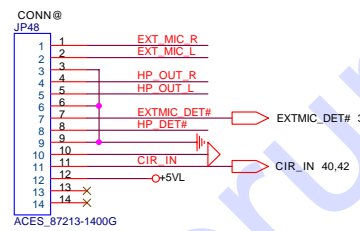
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Issued Date	2006/02/13	Deciphered Date	2006/03/10
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Size			MDC 1.5 & Robson	
Custom	Document Number	Rev		
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0906 Change
3/28 from
NC7SZ04P5X_SC70-5
change to 2N7002

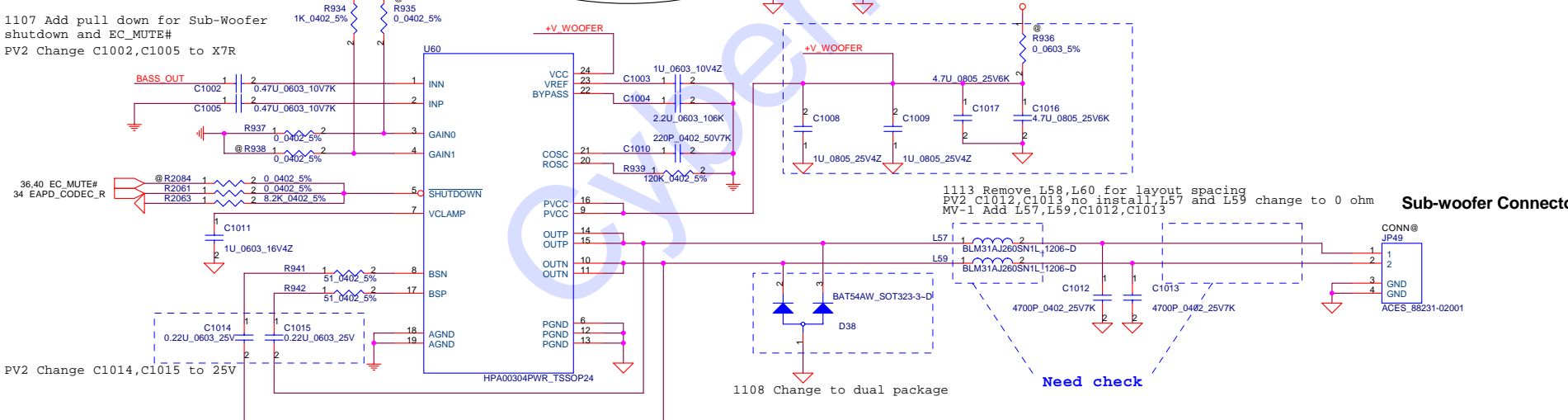
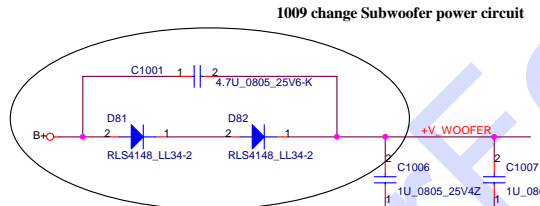
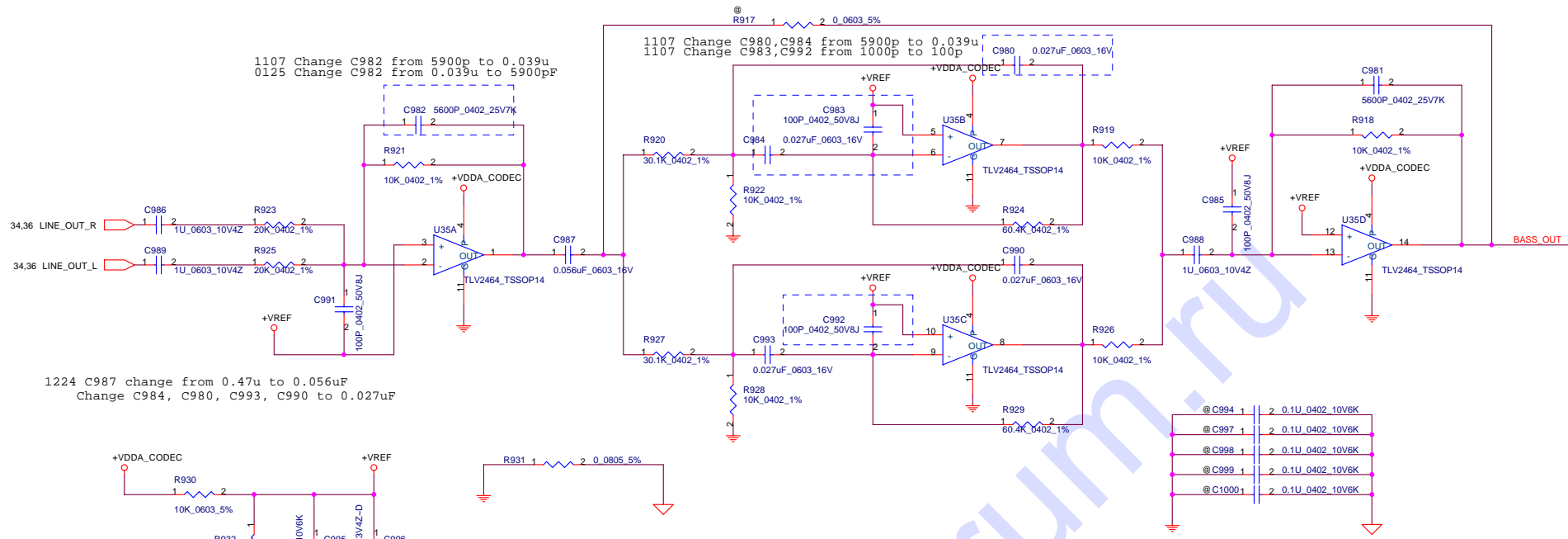


0906 Change pin define
Audio & USB board conn

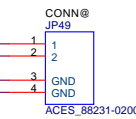


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Compal Electronics, Inc.		
AMP & Audio Jack		
Title	Document Number	
Size	LA-4082P Vader Discrete	
Custom	Date: Tuesday, April 29, 2008	
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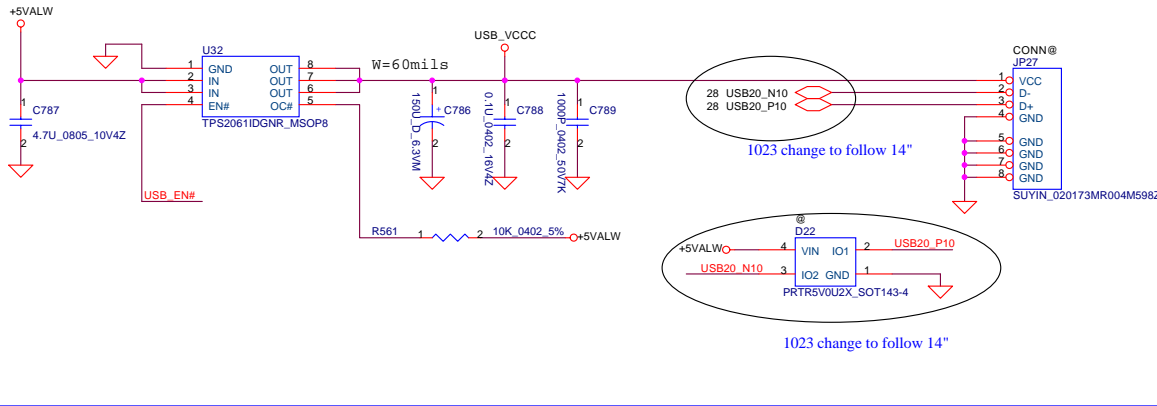
Sub-woofer Connector



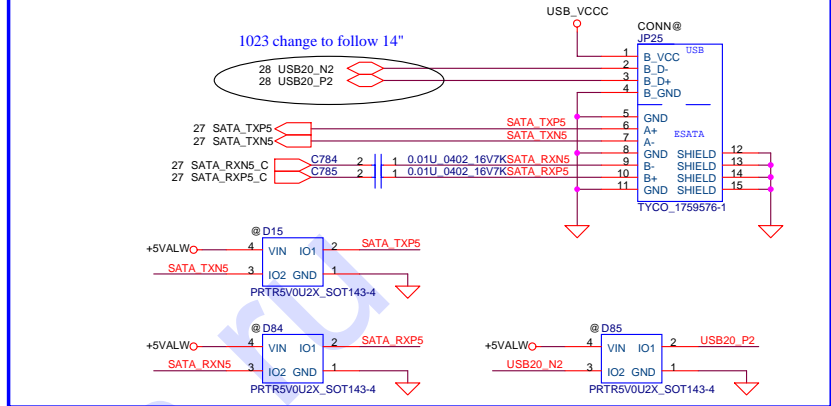
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Issued Date	2006/02/13	Deciphered Date
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Title		Compal Electronics, Inc.	
		EQ & Sub Woofer	
Size	Document Number		Rev
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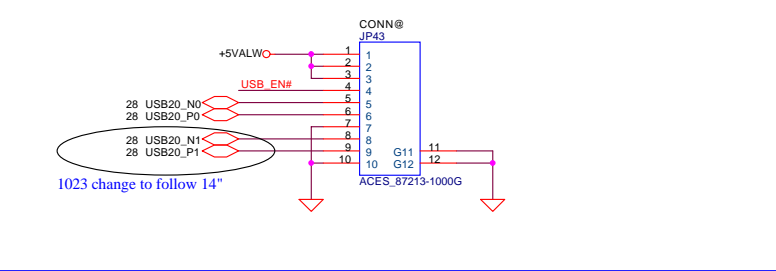
Left side USB Connector



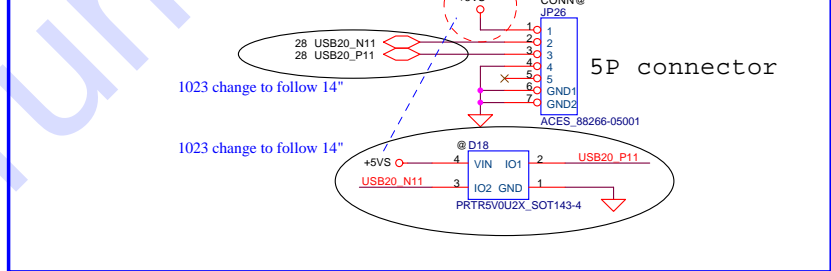
Left side ESATA/USB combination Connector



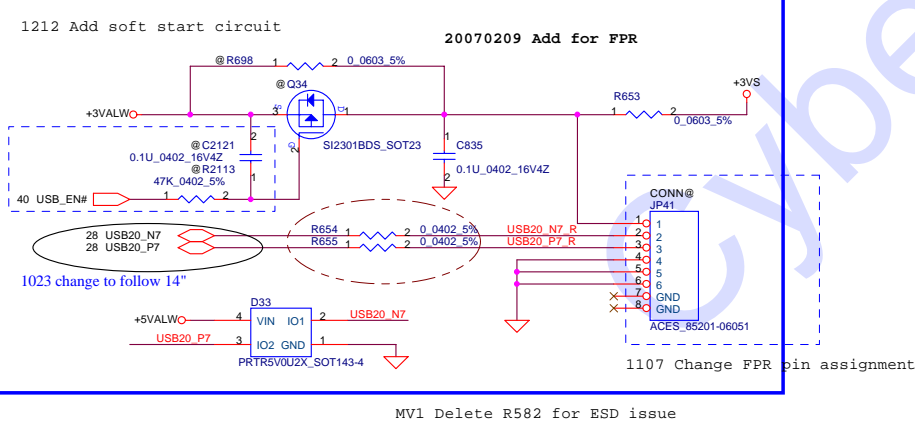
USB cable connector for Right side



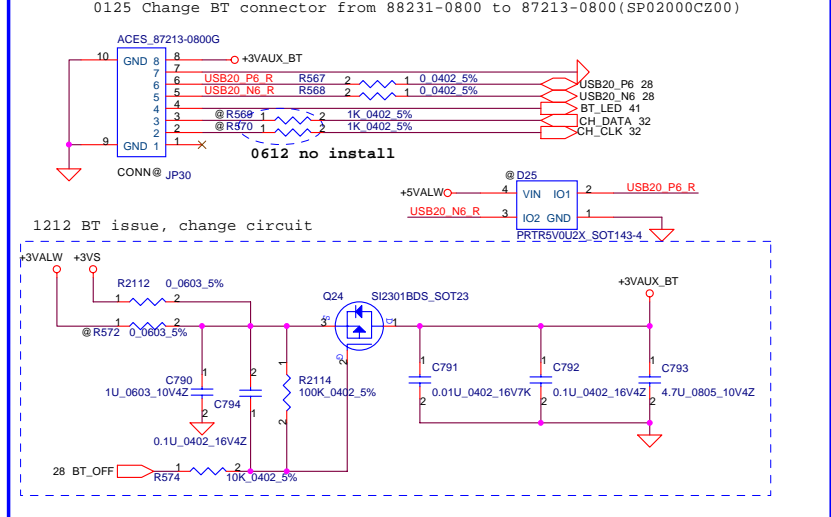
Touch screen connector



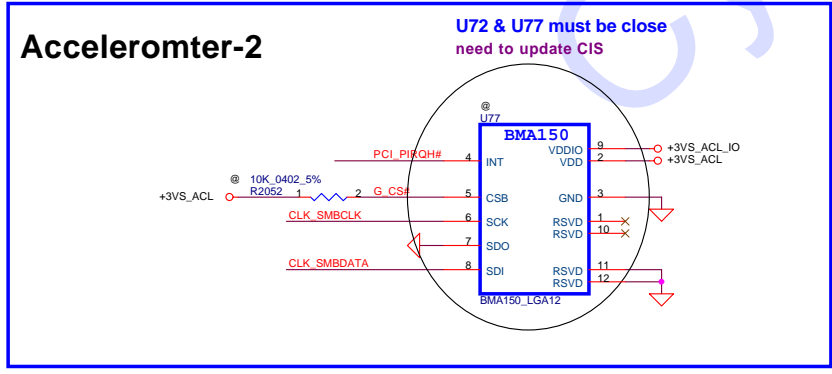
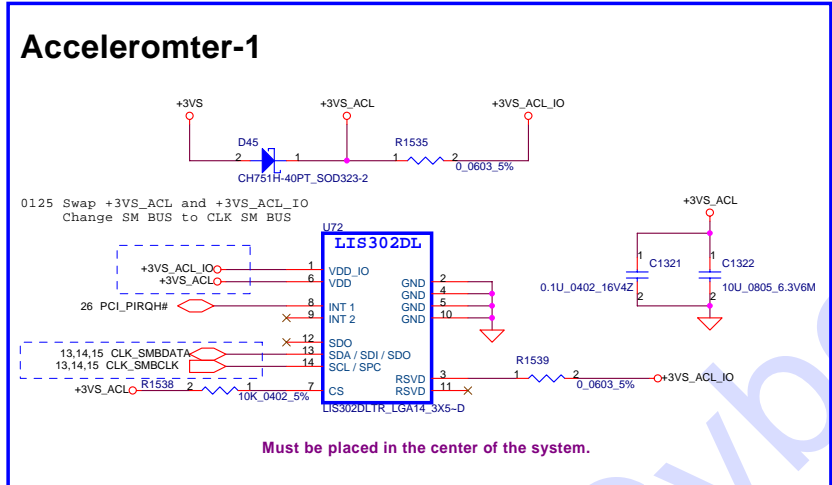
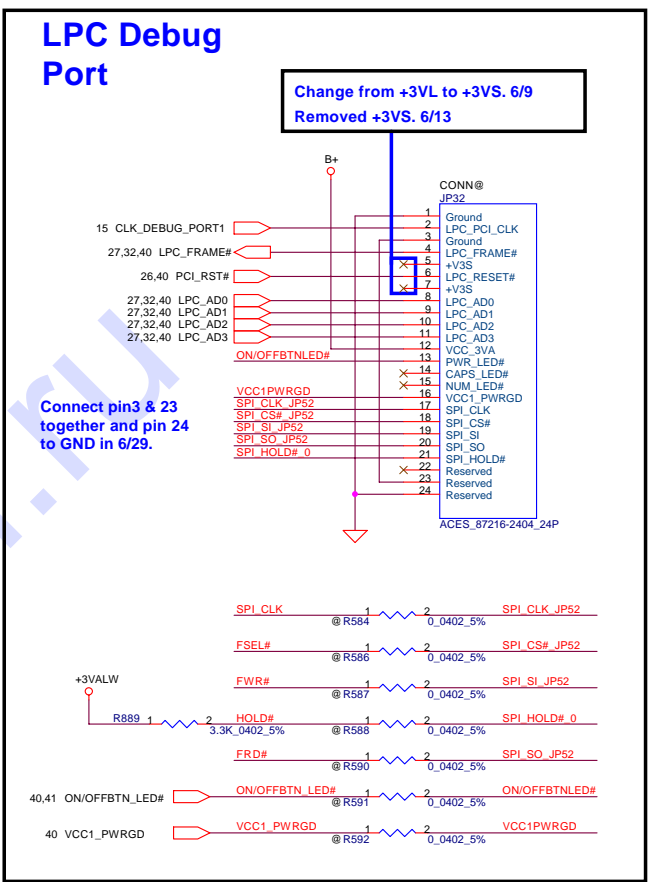
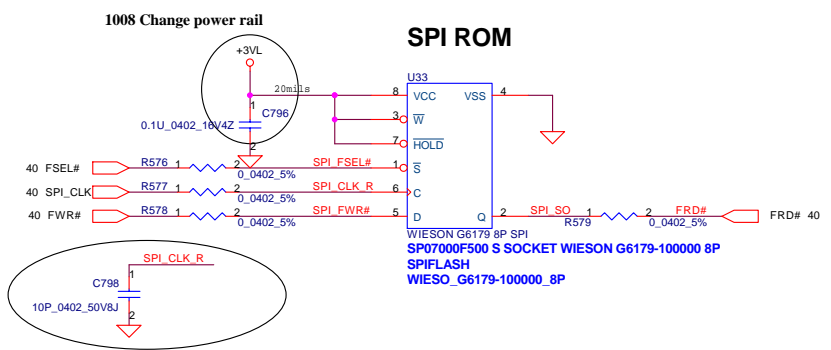
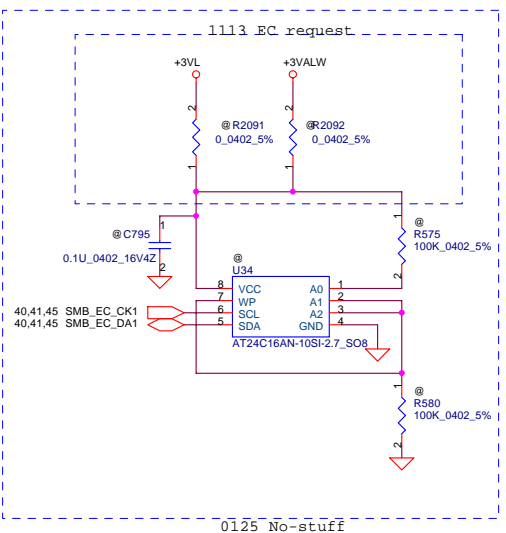
Finger printer



BT Connector

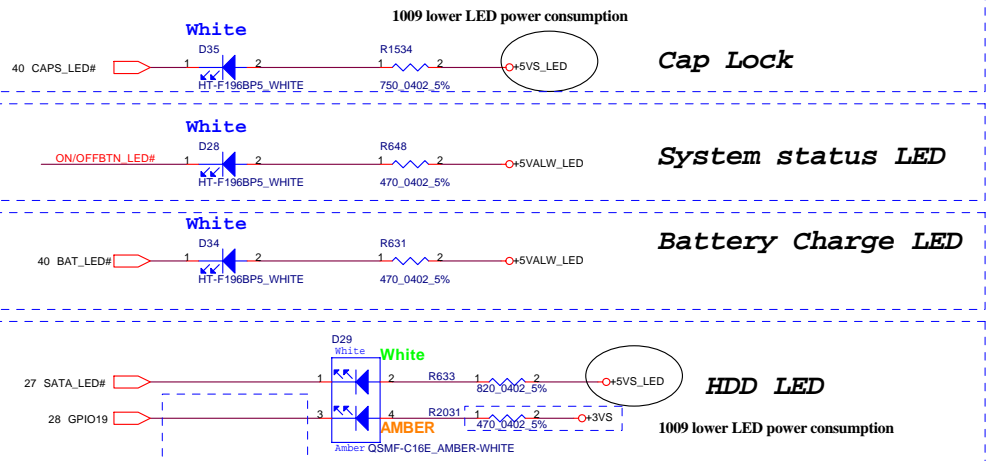


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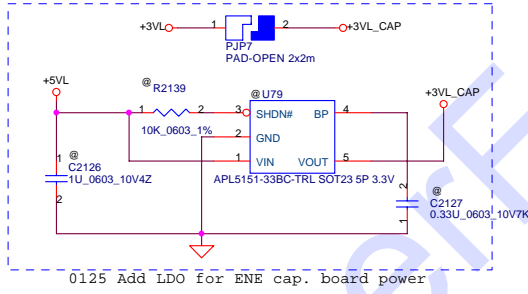
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Size	Document Number	Date		Sheet	Rev
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LED

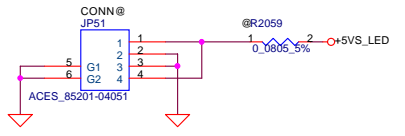


1025 change to follow IBT00 design
 1102 Change GSENSOR LED control pin from SB to KBC
 1106 Delete R668, control by SB

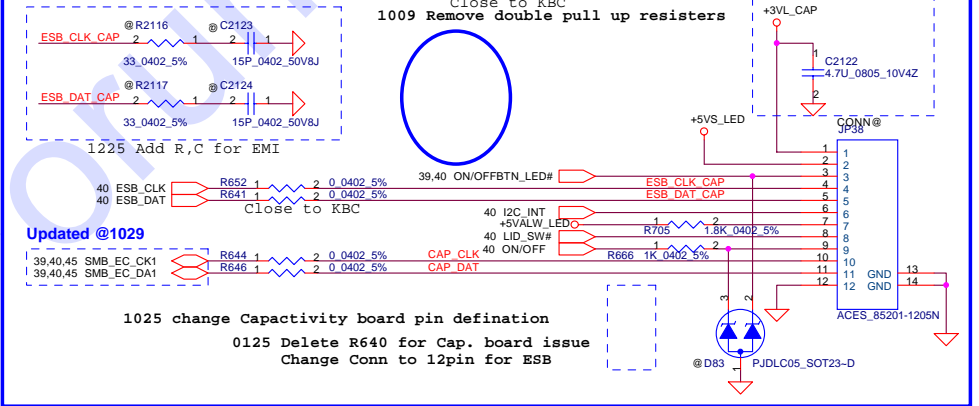
for debug only
 1212 Delete SW5, SW6



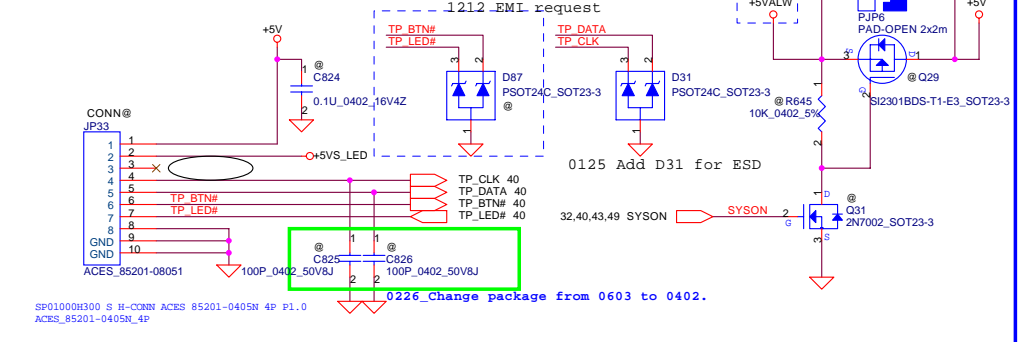
K/B backlight



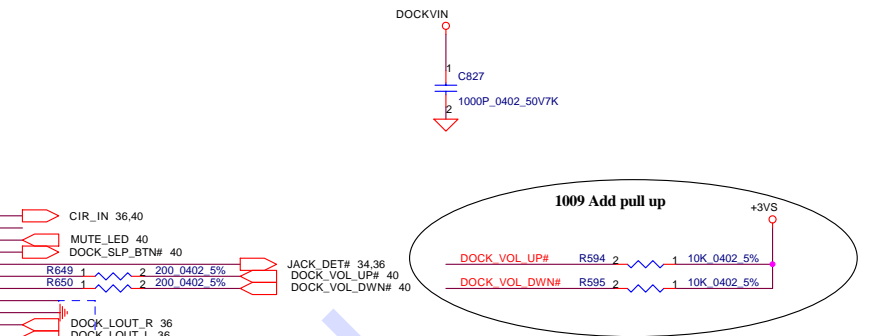
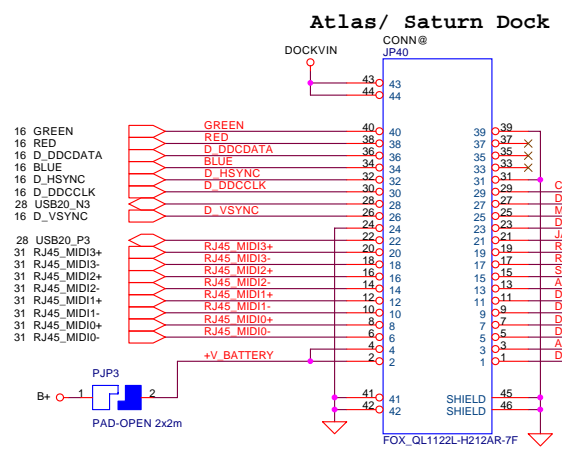
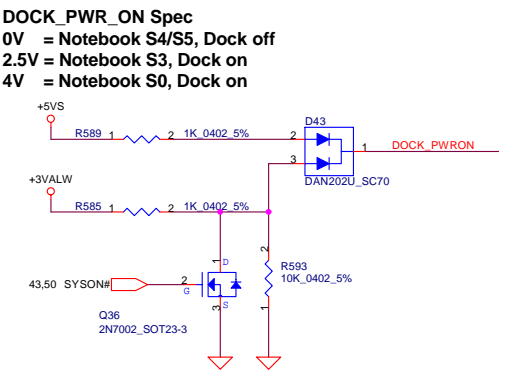
SWITCH BOARD.



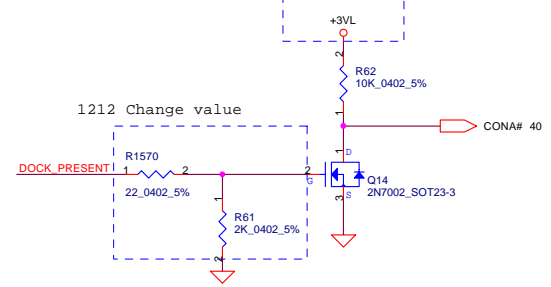
T/P Board (Inculde T/P_ON/OFF)



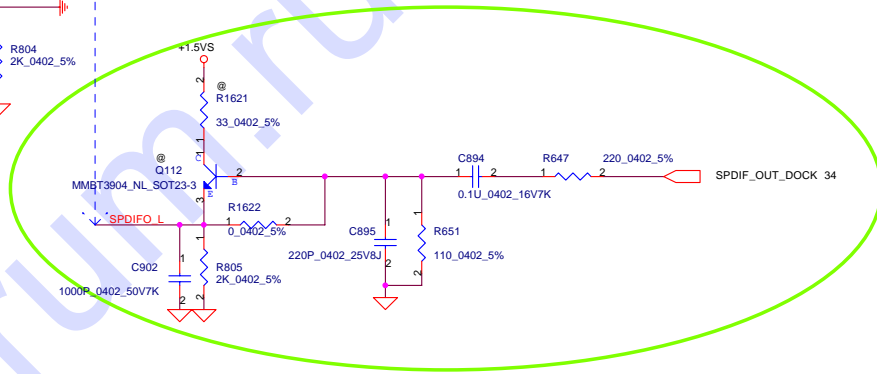
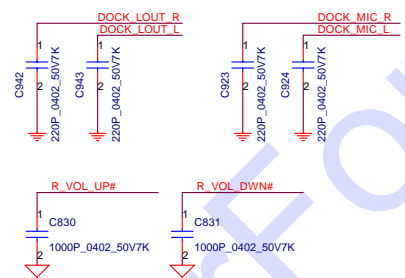
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Issued Date	2006/02/13	Deciphered Date	2006/03/10	KBD, ON/OFF, SW, CIR	
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Custom	LA-4082P Vader Discrete	0.1			



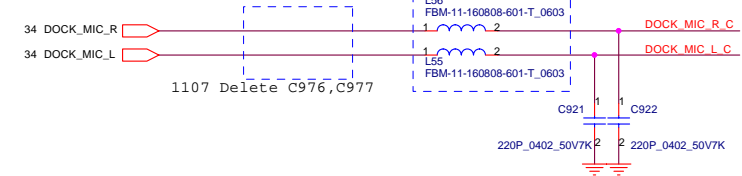
1112 Change power rail from +3VALW to +3VL



need change to reverse type connector



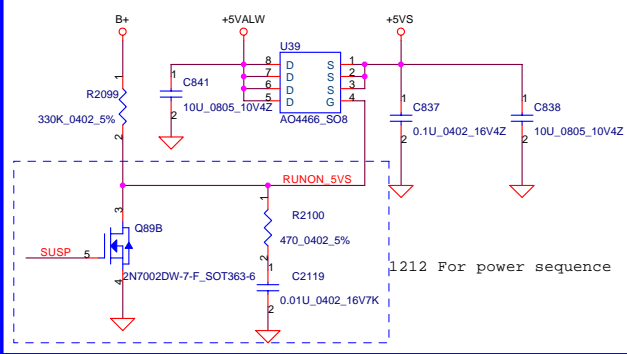
MIC_Dock



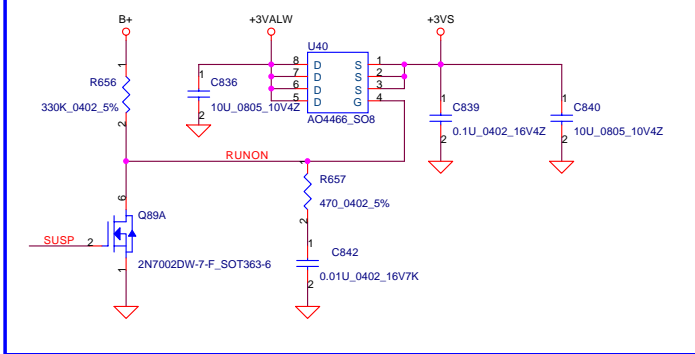
1009 Remove TV components

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Size	Document Number	Rev		0.1
Custom	LA-4082P Vader Discrete			
Date:	Tuesday, April 29, 2008	Sheet	42 of 61	

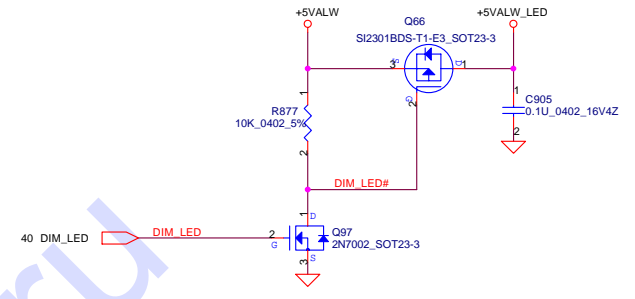
+5VALW to +5VS Transfer



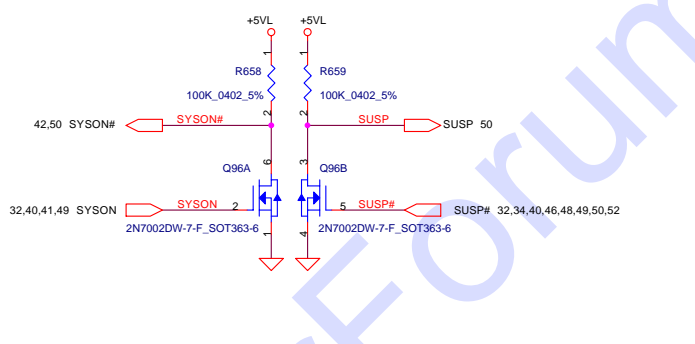
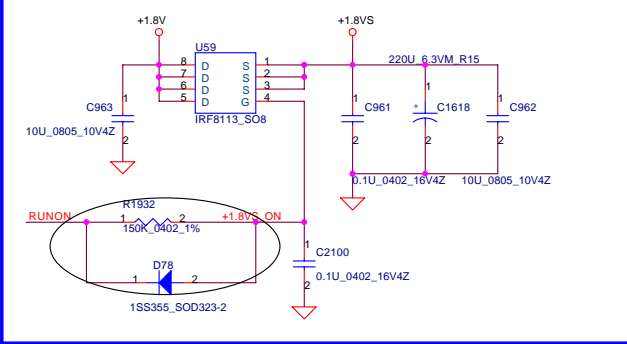
+3VALW to +3VS Transfer



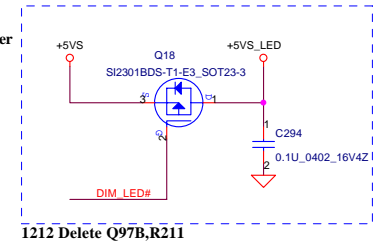
DIMM LED



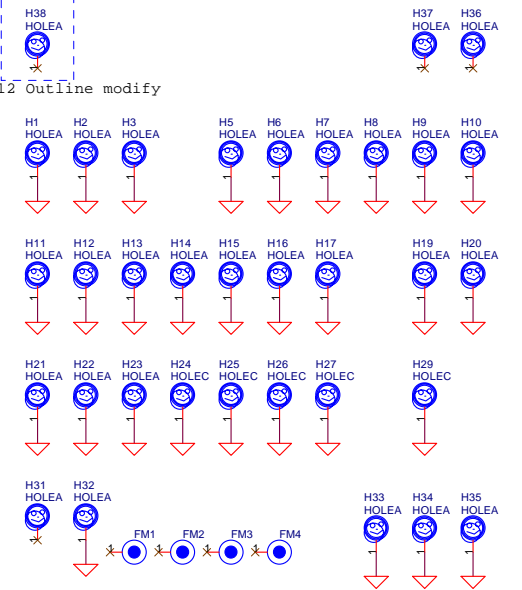
+1.8V to +1.8VS Transfer



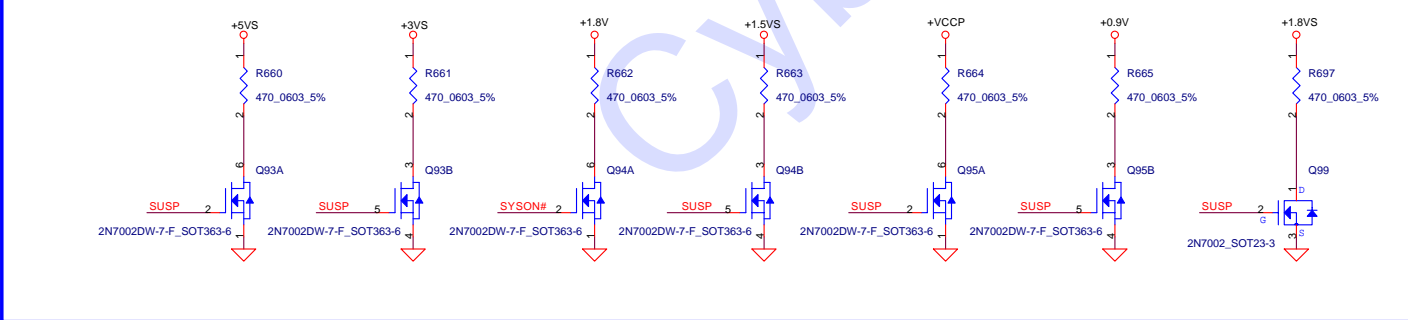
1009 Add for LED power



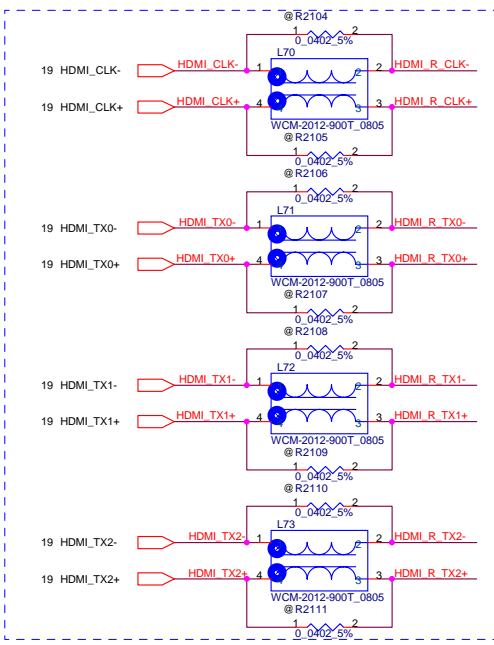
1212 Outline modify



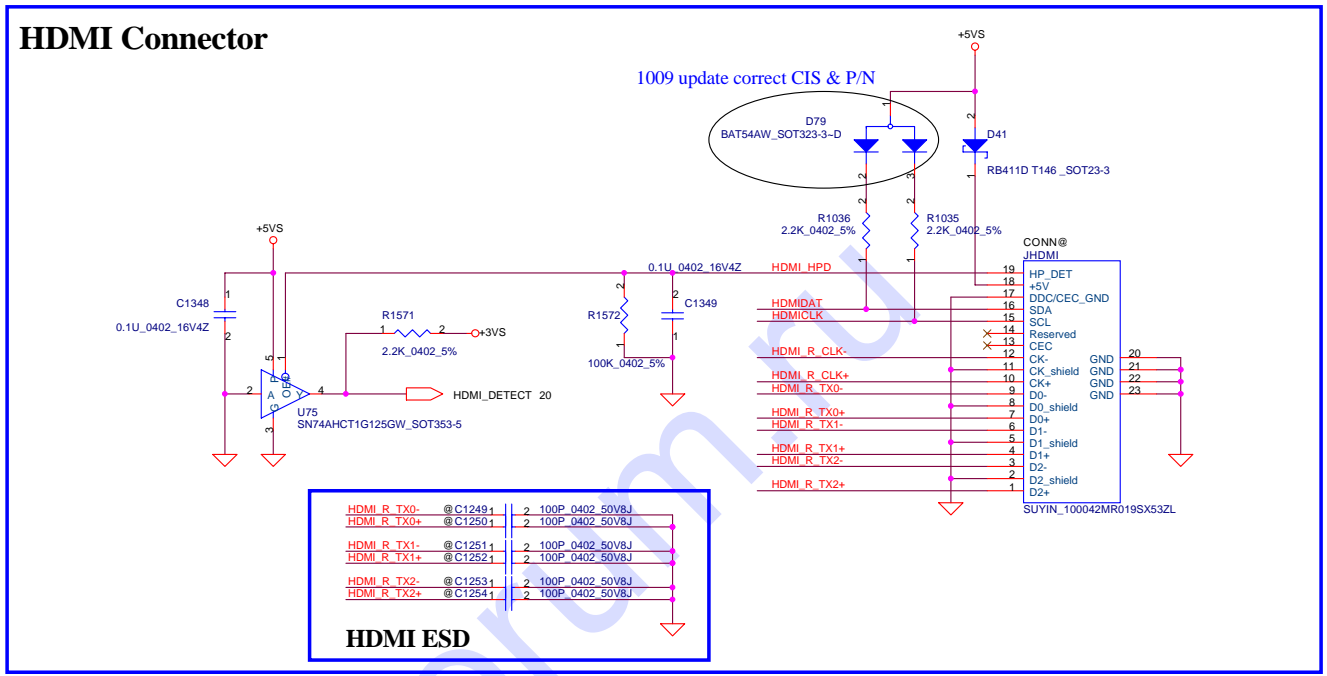
Discharge circuit



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				Custom	LA-4082P Vader Discrete
				Date:	Tuesday, April 29, 2008
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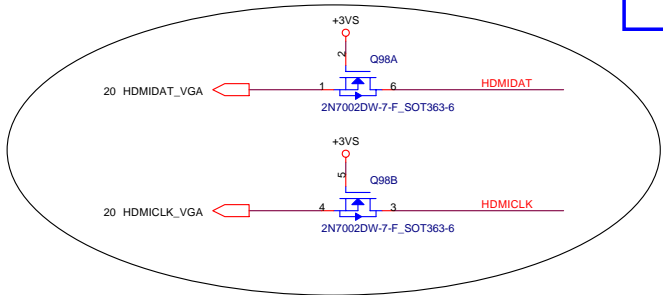


HDMI Connector



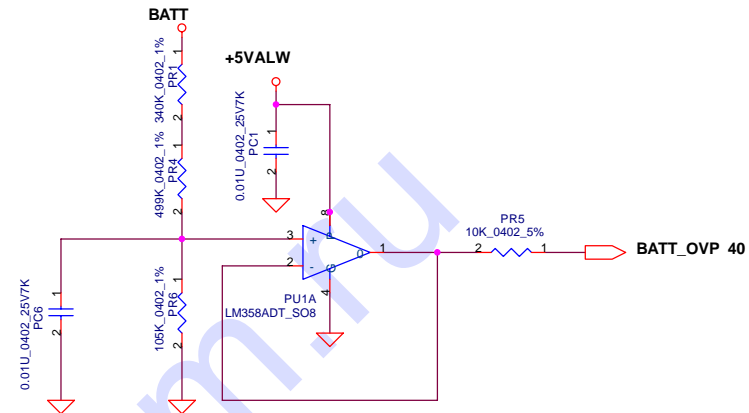
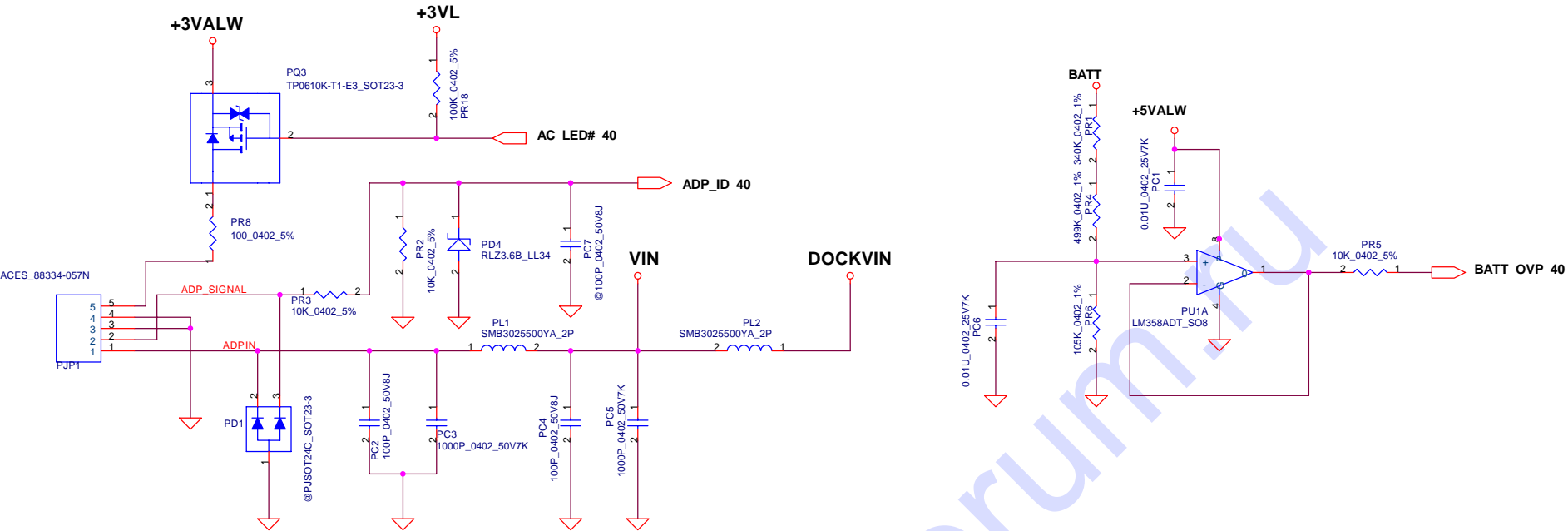
HDMI ESD

HDMI_R_TX0-	@ C1249-4	2	100P	0402	50V8J
HDMI_R_TX0+	@ C1250-1	2	100P	0402	50V8J
HDMI_R_TX1-	@ C1251-1	2	100P	0402	50V8J
HDMI_R_TX1+	@ C1252-1	2	100P	0402	50V8J
HDMI_R_TX2-	@ C1253-1	2	100P	0402	50V8J
HDMI_R_TX2+	@ C1254-1	2	100P	0402	50V8J

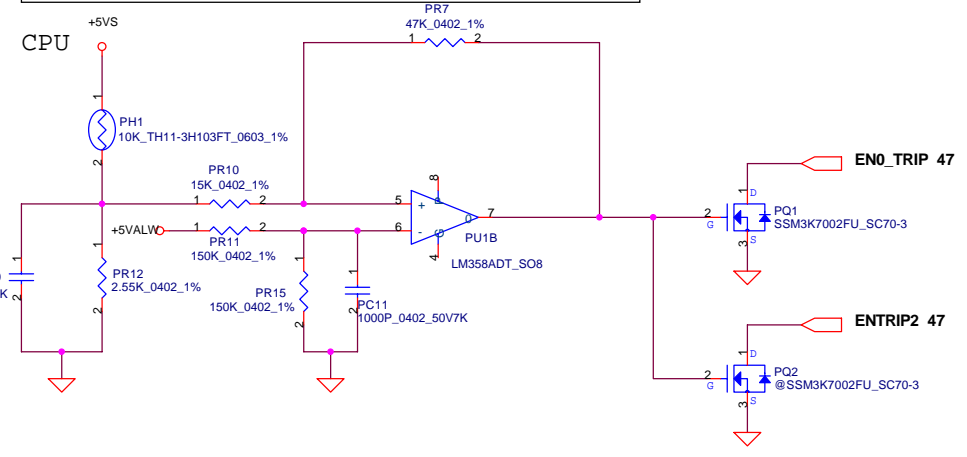
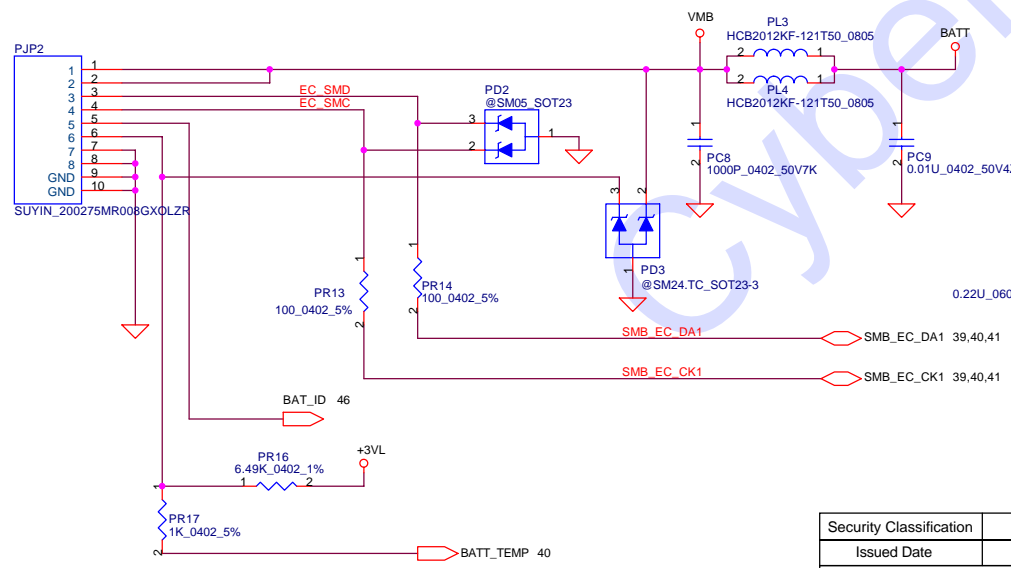


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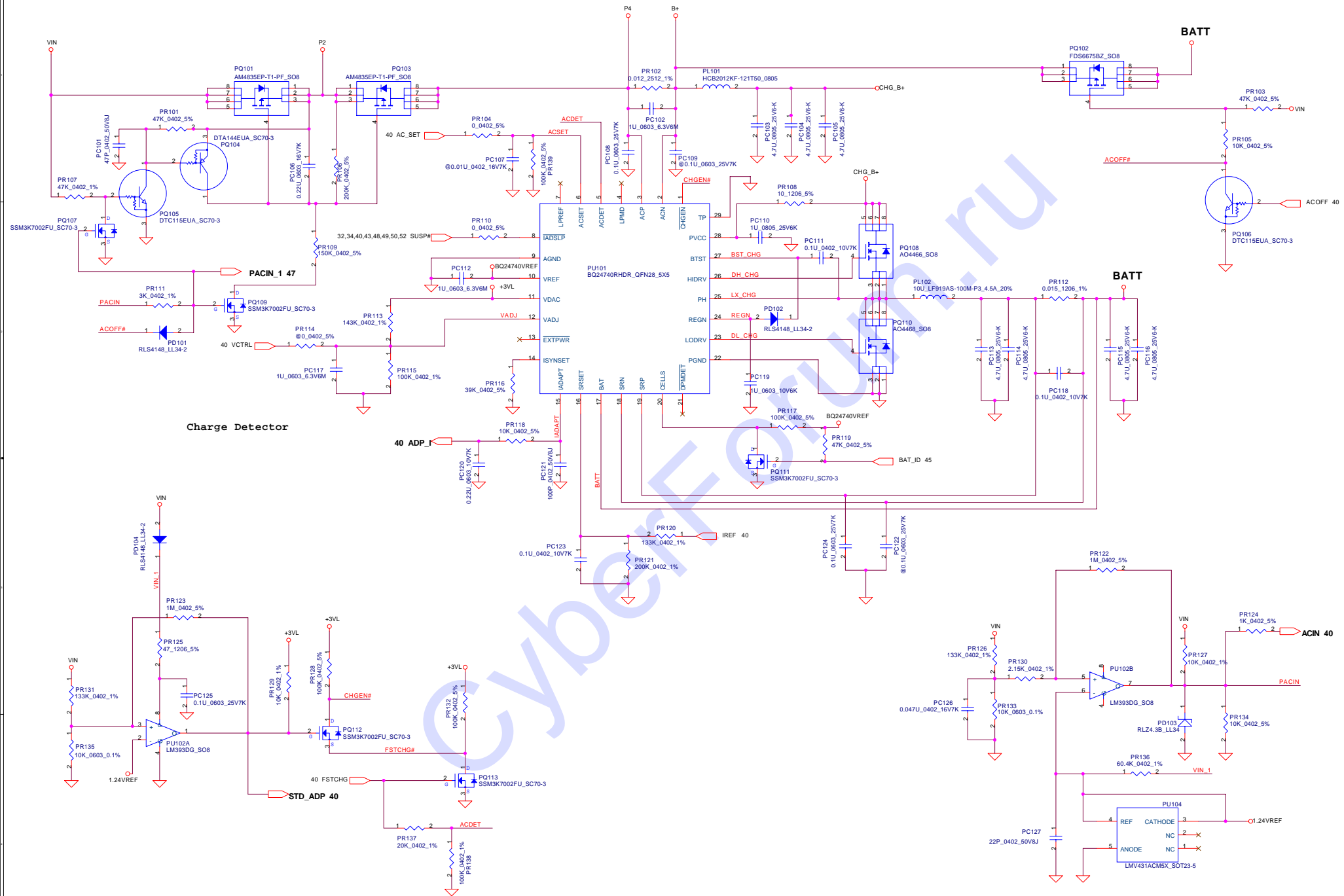
Title		Compal Electronics, Inc.	
		HDMI LS & Conn.	
Size	Document Number	Date	Rev
Custom	LA-4082P Vader Discrete	Tuesday, April 29, 2008	0.1
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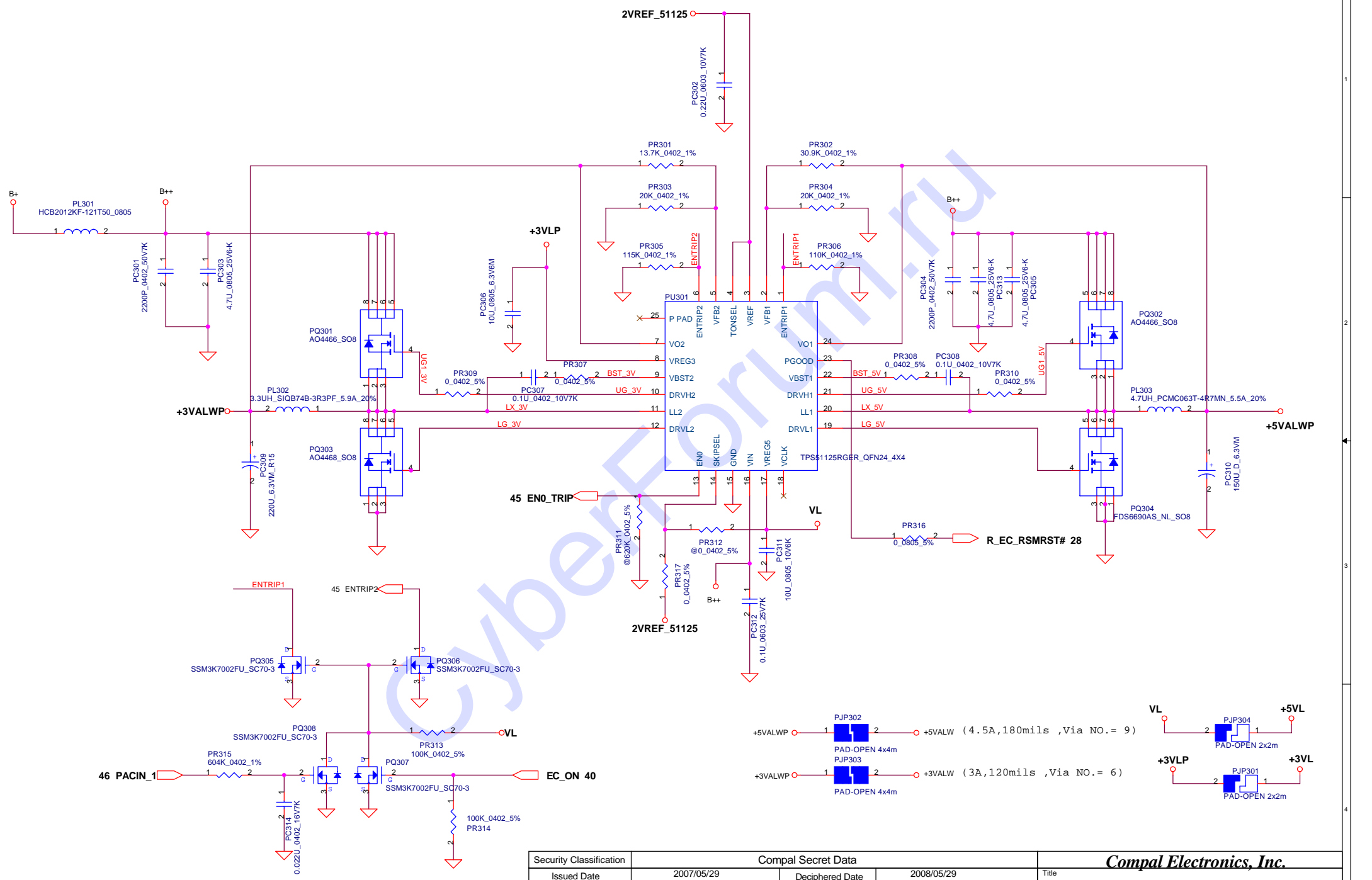
PH1 under CPU bottom side :
 CPU thermal protection at 90 +-3 degree C
 Recovery at 47 +-3 degree C



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Size	Document Number	Montevina Consumer Discrete		Rev	0.1
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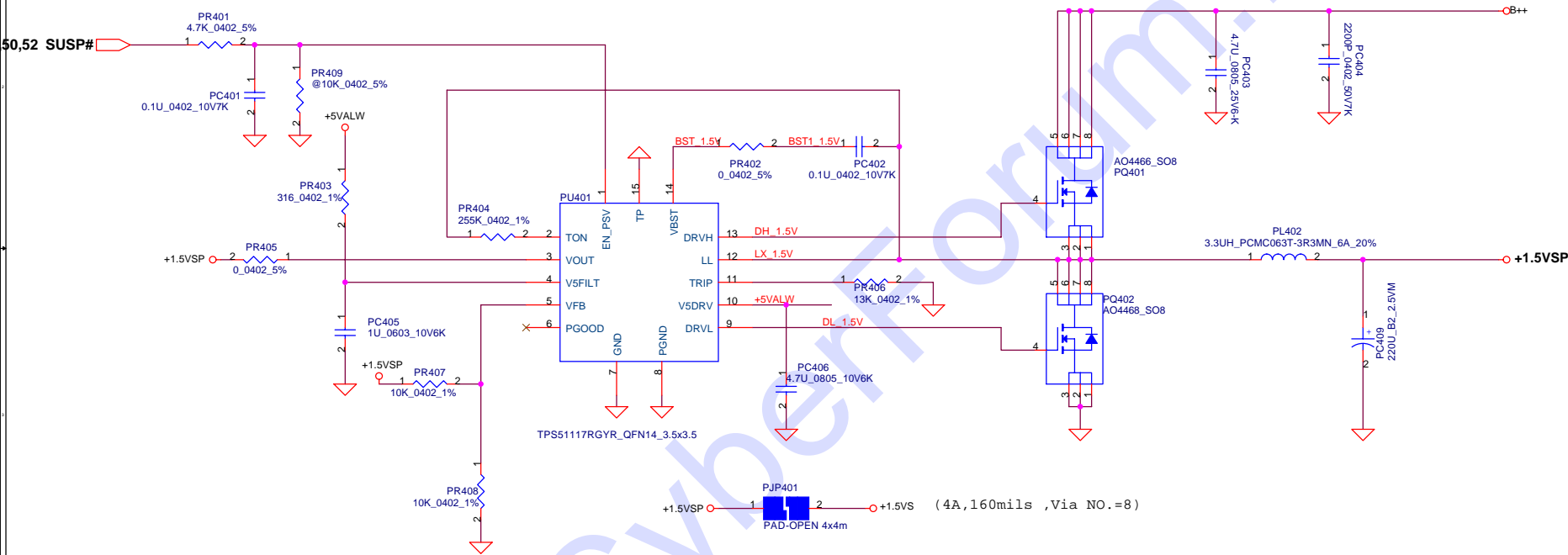
Security Classification		Compal Secret Data		Title	
Issued Date	2007/05/29	Deciphered Date	2008/05/29	3.3VALWP/5VALWP	
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Date:	Tuesday, April 29, 2008	Sheet	47	of	52

Compal Electronics, Inc.

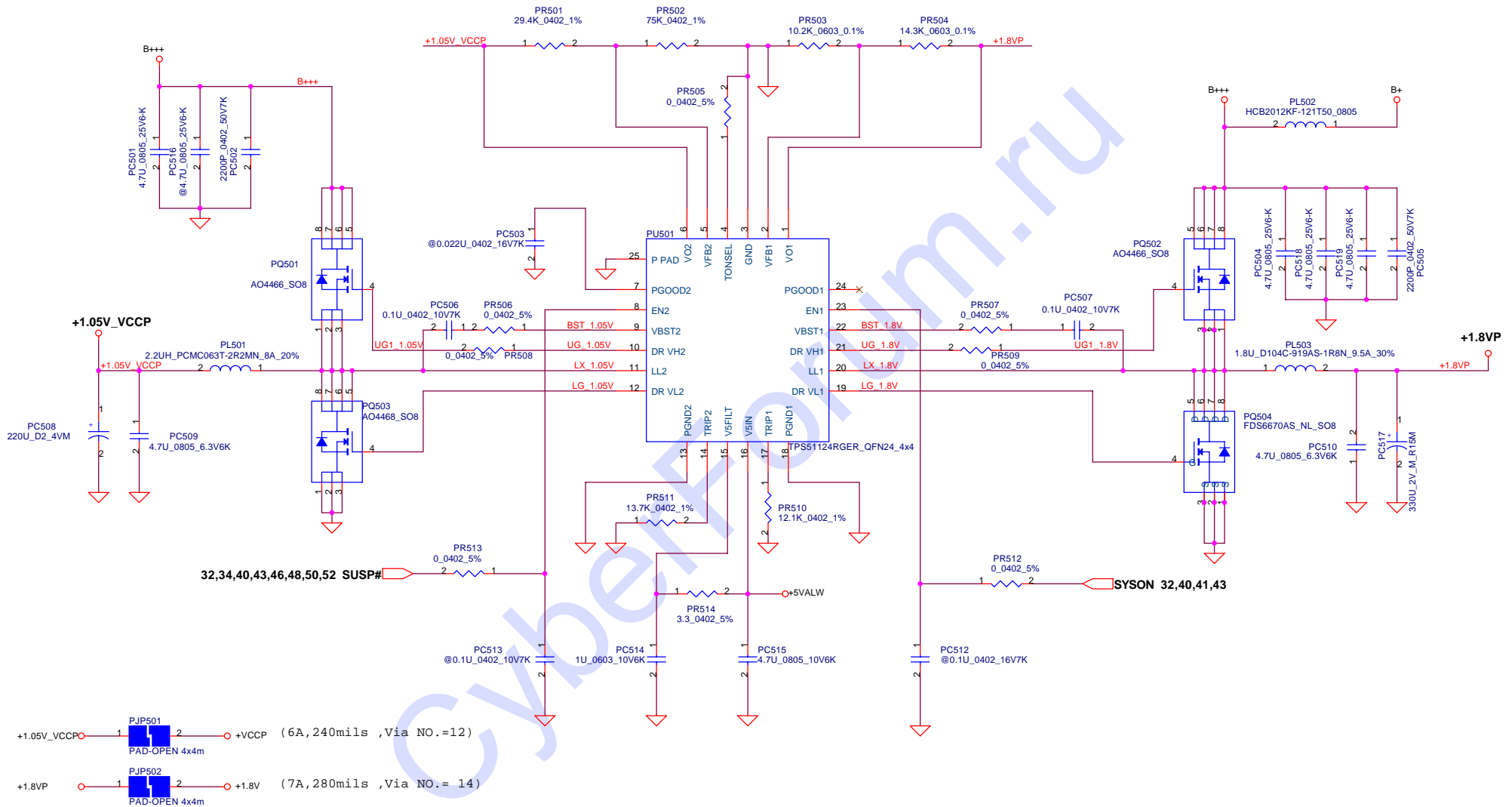
3.3VALWP/5VALWP

Montevina Consumer Discrete

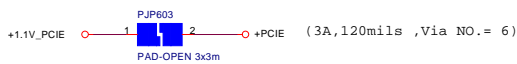
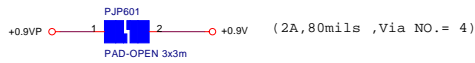
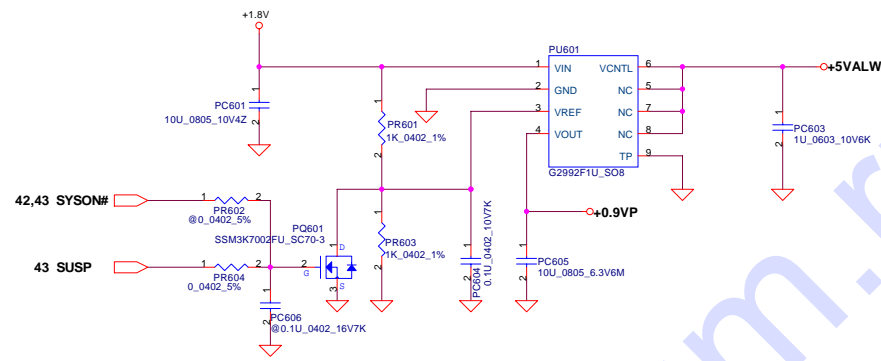
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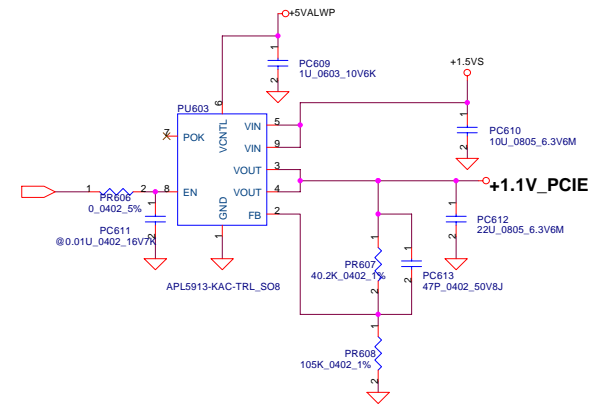
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				Size	Document Number
Date: Tuesday, April 29, 2008				Sheet	48 of 52



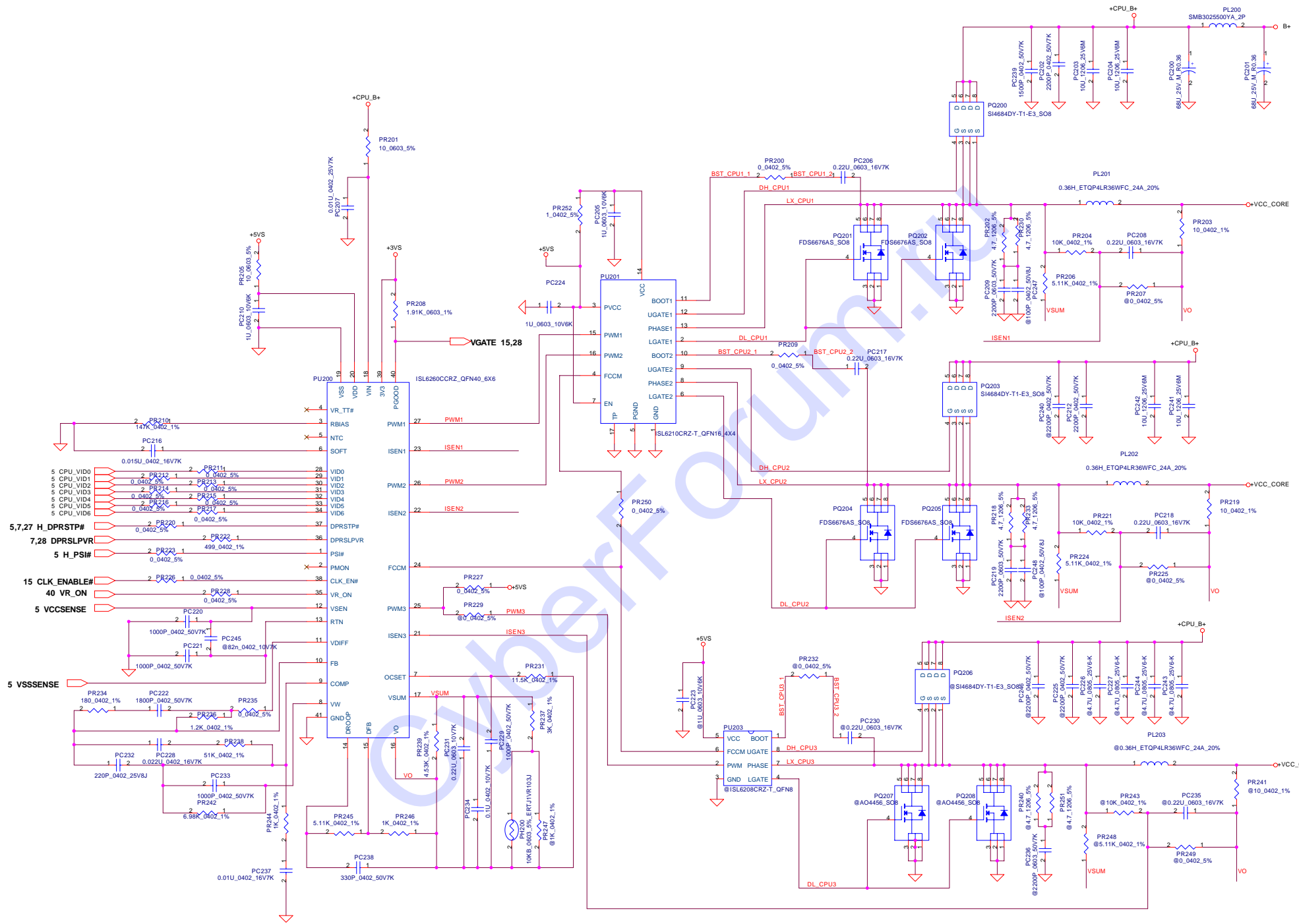
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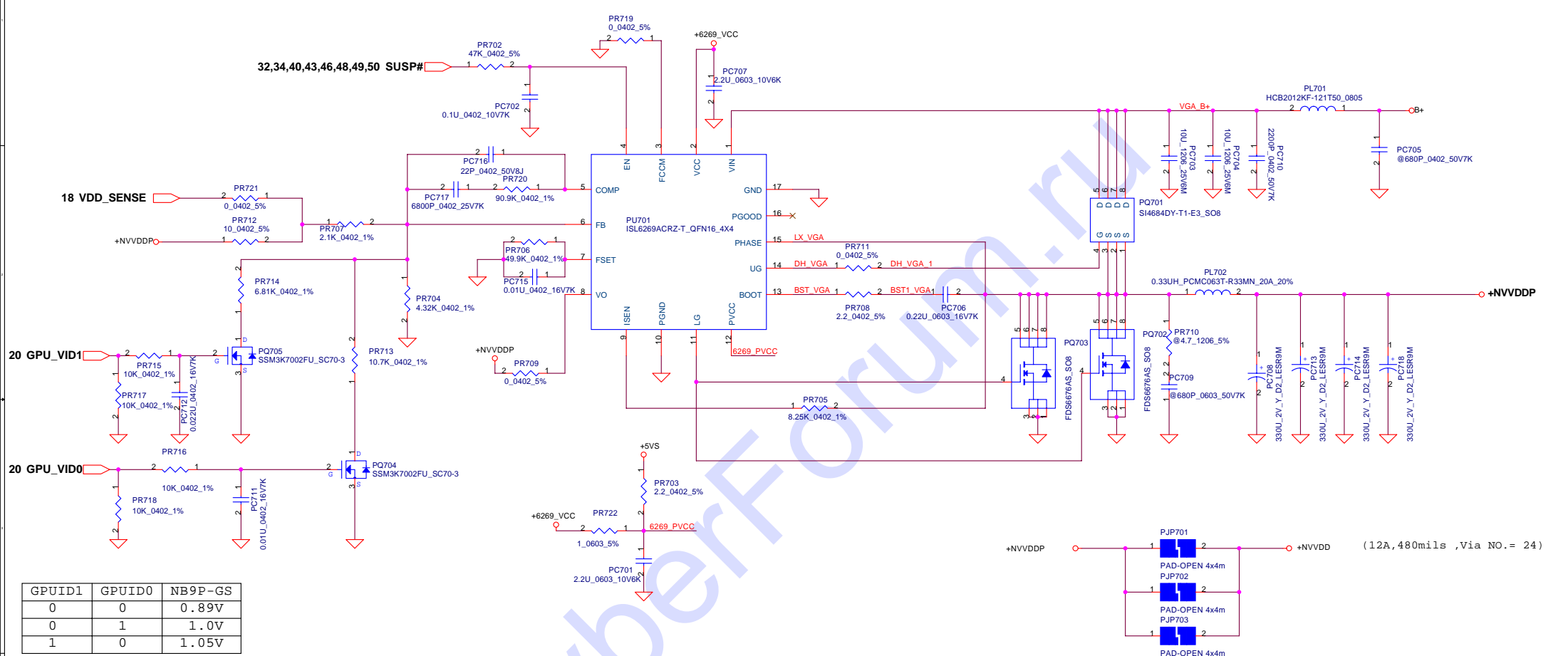
32,34,40,43,46,48,49,52 SUSP#



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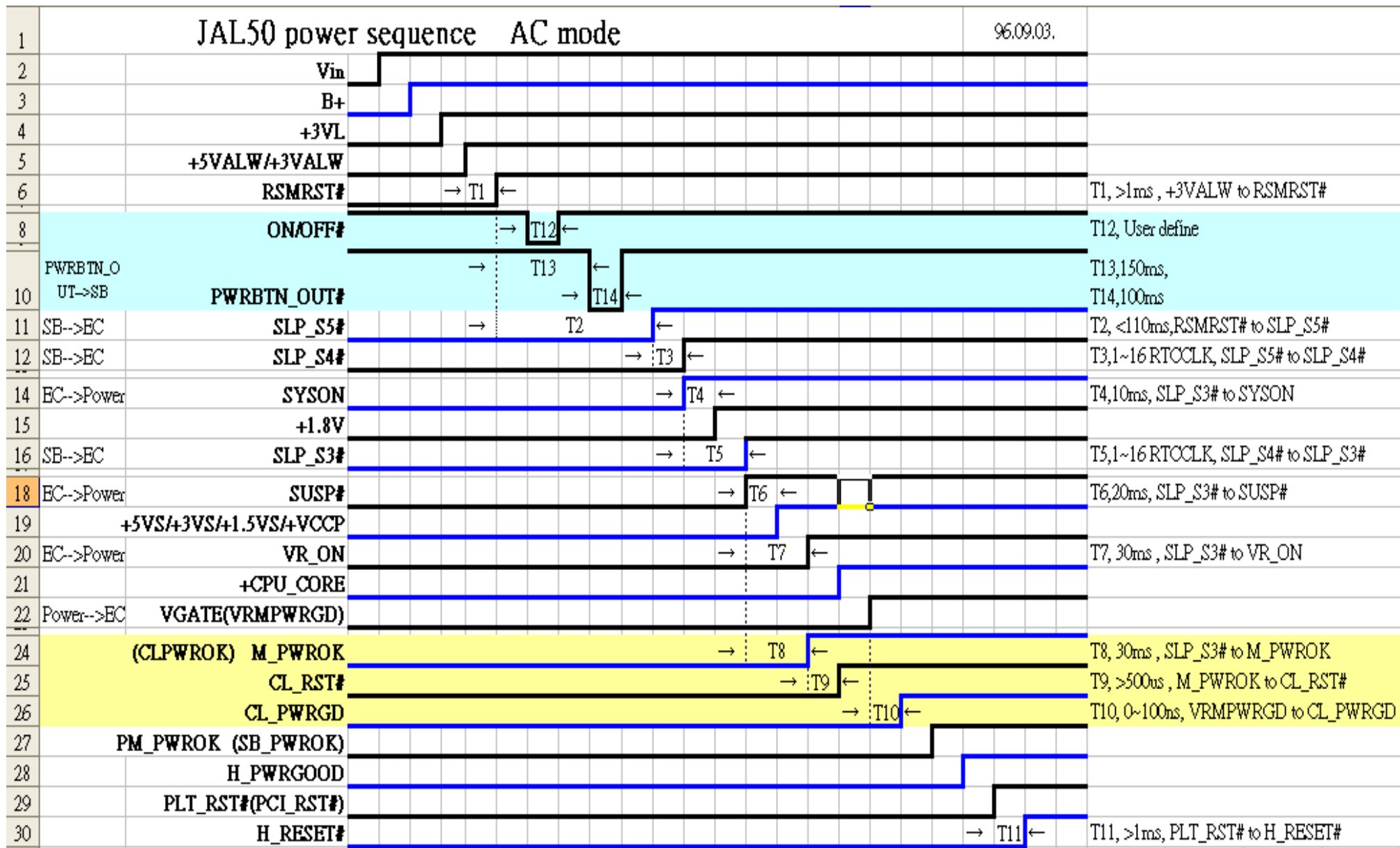


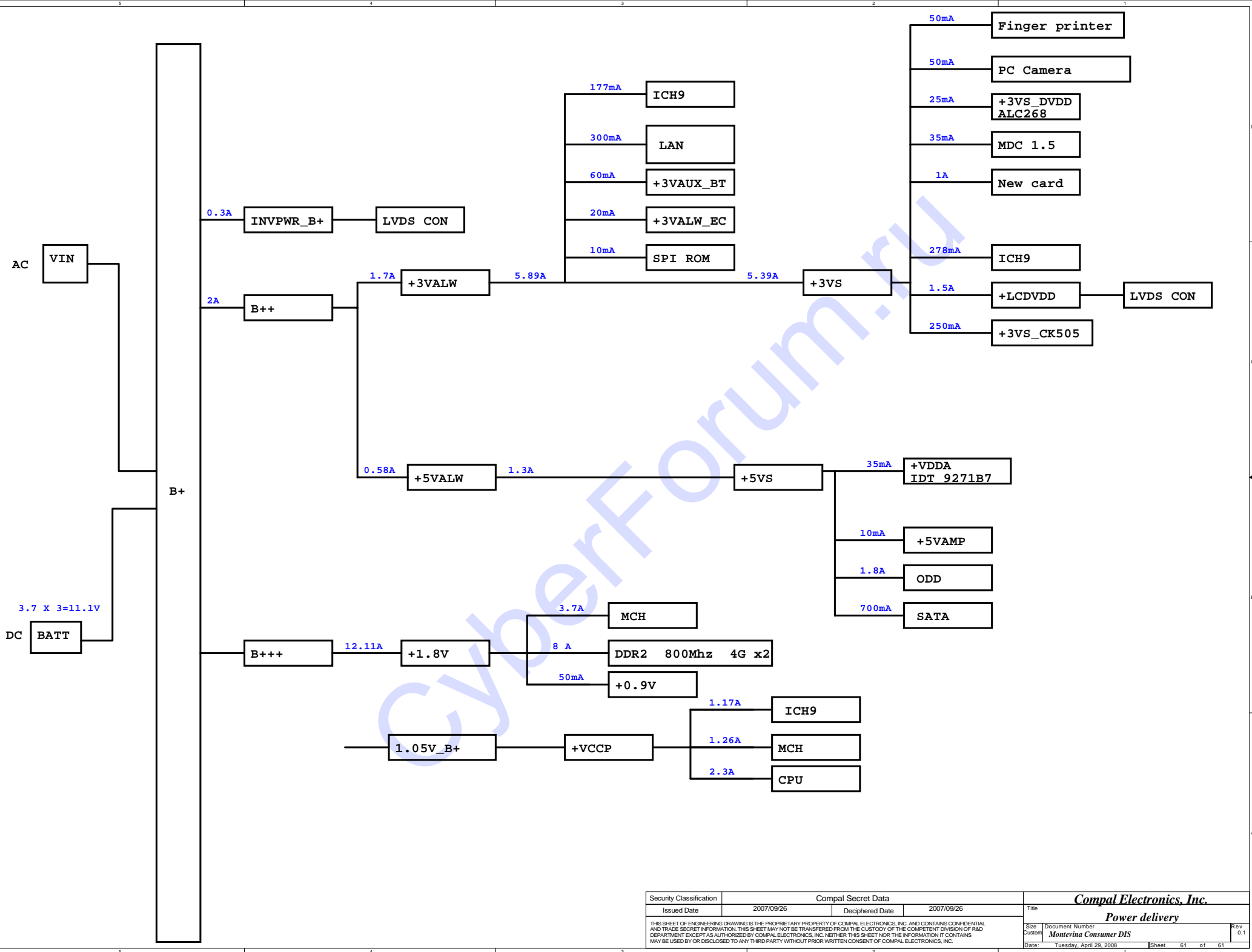
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				CPU CORE
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GPUVID1	GPUVID0	NB9P-GS
0	0	0.89V
0	1	1.0V
1	0	1.05V

+NVVDDP	PJP701	2	+NVVDD	(12A, 480mils, Via NO. = 24)
	PAD-OPEN 4x4m			
	PJP702	2		
	PAD-OPEN 4x4m			
	PJP703	2		
	PAD-OPEN 4x4m			





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				Rev: 0.1
			Sheet: 61 of 61	