

COMPAL CONFIDENTIAL

MODEL NAME : LOKI 15/17
 PCB NO : DA6001TR010
 BOM P/N : 431A7X31L01~L07

KBL-U & R + MEC1416 board 2017-07-26

REV : 1.0 (A00)

zzz **PCB R1**
 DAZ21Q00101
 PCB@
 PCB CAL60 LA-F114P LS-F111P GOLD A31 !


SKL
 UC1
 SKL_U SA0000ACL1L
 i3SKL_2.0G_SMB0@
 S IC FJ8066201931106 SR2UW D1 2G A31!

KBL
 UC1
 KBL_U_Celeron SA0000ADL3L
 KBL_U_Celeron@
 S IC FJ8067702739933 SR349 H0 1.8G A31!
 UC1
 KBL_U_Pentium SA0000ADV3L
 KBL_U_Pentium@
 S IC FJ8067702739932 SR348 H0 2.3G A31!
 UC1
 KBL_U_i3 SA0000A380L
 KBL_U_i3@
 S IC A31 FJ8067702739738 QLDP H0 2.4G
 UC1
 KBL_R_i5 SA0000AWB3L
 i5KBLR_1.6G_QS@
 S IC FJ8067703282221 SR3LB Y0 1.6G A31!
 UC1
 KBL_R_i7 SA0000AQZ0L
 i7KBLR_1.8G_ES@
 S IC A31 FJ8067703281813 QN5C Y0 1.8G
 UC1
 KBL_R_i7 SA0000AWC2L
 i7KBLR_1.8G_QS@
 S IC FJ8067703281816 SR3LC Y0 1.8G A31!
 UC1
 KBL_U_i3 SA0000B2Y1L
 i3KBLU_2.7G_QS@
 S IC FJ8067702739765 SR3JY H0 2.7G A31!

@ : Un-pop Component
 UMA@/DIS@ : UMA & DIS Type
 U22@/U42@ : KBL U/KBL U-R
 EC@ : EC
 JP@/PJP@ : JUMP

EMI@/ESD@/RF@ : EMI, ESD and RF Component
 @EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
 CMC@ : XDP Component
 CONN@ : Connector Component
 TP_WAKE@/NTP_WAKE@ : TouchPad wake
 KBBL@ : KB Backlight
 TPM@/FTPM@ : HW TPM/SW TPM
 MMC@ : eMMC
 FFS@ : Free Fall Sensor
 MODS@ : Modern Standby

Layout Dell logo



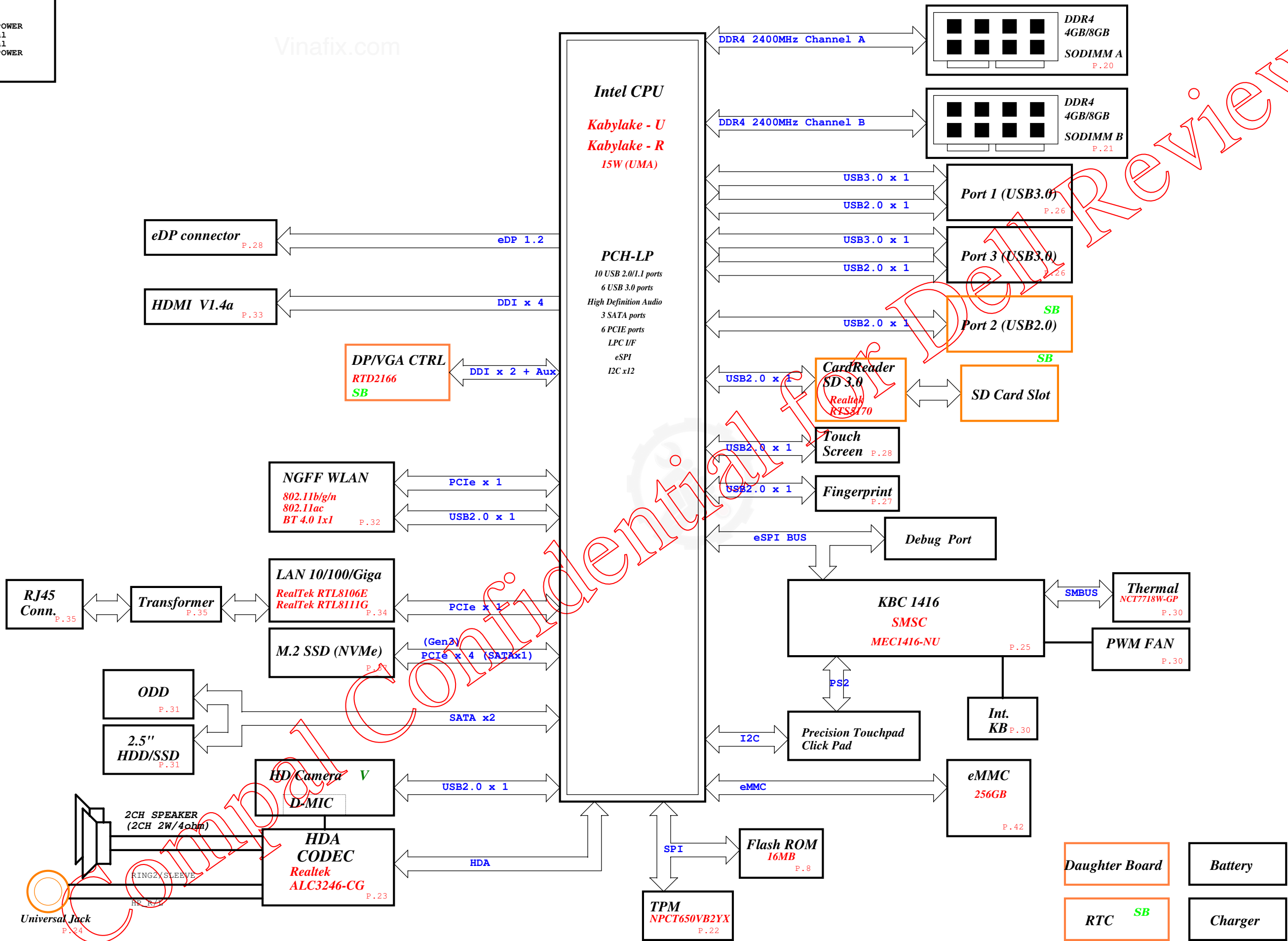
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 REV: X00
 PWB: 9HTP8

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PCB Stack
1.0mm/6L
L1:TOP
L2:GND/POWER
L3:Signal
L4:Signal
L5:GND/POWER
L6:BOT

Block Diagram

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF

USB PORT#	DESTINATION
1	USB2.0 Port1
2	USB2.0 Port2 , IO/B
3	USB2.0 Port3
4	NC
5	CCD
6	Card Reader IO/B
7	BT
8	Touch Screen
9	Finger Printer
10	NC

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1			USB3.0 Port1
USB3.0-2			NC
USB3.0-3			USB3.0 Port3
USB3.0-4			NC
USB3.0-5	PCIE-1		NC
USB3.0-6	PCIE-2		NC
	PCIE-3		NC
	PCIE-4		NC
	PCIE-5		10/100M LAN
	PCIE-6		WLAN
	PCIE-7	SATA-0	SATA HDD
	PCIE-8	SATA-1	SATA QDD
	PCIE-9		NVME SSD
	PCIE-10		NVME SSD
	PCIE-11	SATA-1*	NVME SSD
	PCIE-12	SATA-2	NVME SSD

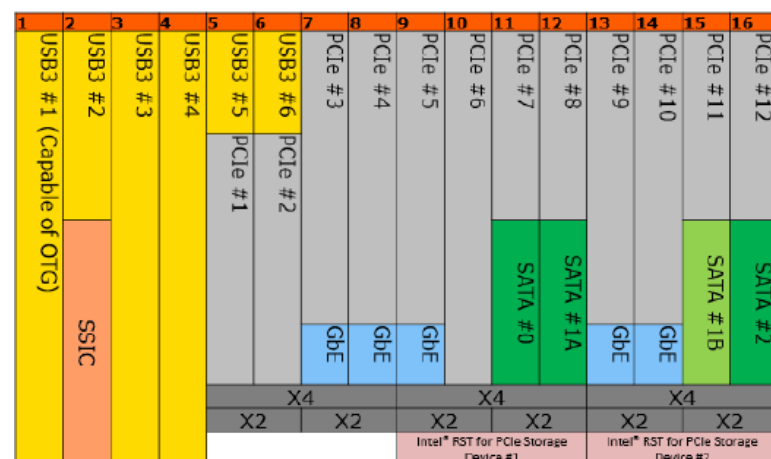
PM TABLE

State \ power plane	+RTC_CELL	B+	+1.0V_PRIM +1.0V_MPHYGT +1.8V_PRIM +3VALW +3VALW_PCH +3.3V_ALW_DSW +5VALW	+1.0V_VCCST +1.2V_DDR +2.5V_MEM	+1.0VS_VCCIO +1.0V_VCCSTG +VCC_GT +VCC_SA +VGA_CORE +VCC_CORE +0.6V_DDR_VTT
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
M3	ON	ON	ON	ON	OFF
S4&S5 / AC	ON	ON	ON	OFF	OFF
S4&S5 / AC doesn't exist	ON	ON	OFF	OFF	OFF
G3	ON	OFF	OFF	OFF	OFF

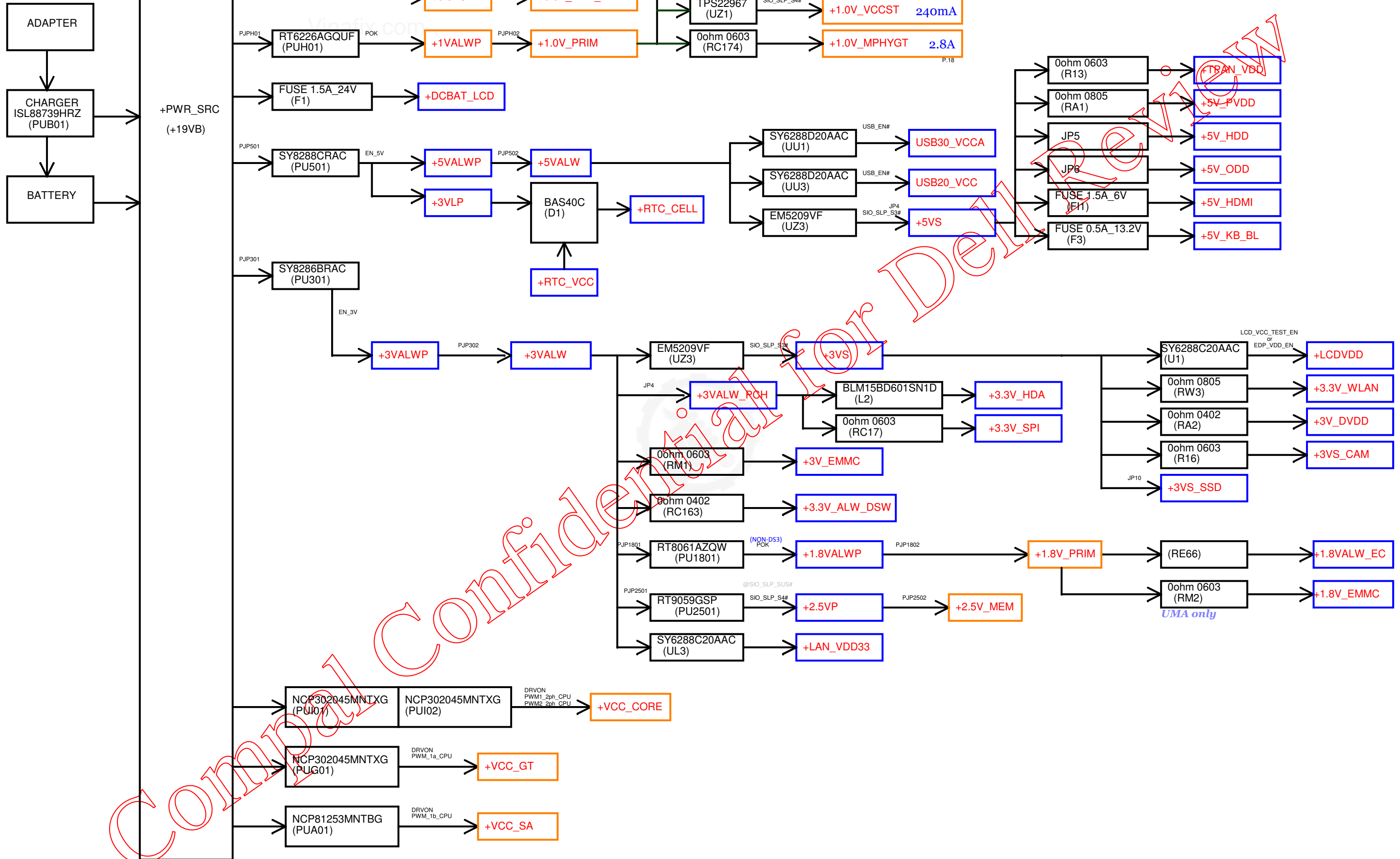
Board ID table

Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10K	3.000	EVT
2	100	17.8K	2.801	DVT1
3	100	27K	2.598	DVT2
4	100	37.4K	2.402	
5	100	49.9K	2.201	Pilot
6	100	64.9K	2.001	
7	100	82.5K	1.808	
8	100	107K	1.594	
9	100	154K	1.299	
10	100	200K	1.1	
11	100	TBD	0.9	
12	100	TBD	0.7	
13	100	TBD	0.5	
14	100	TBD	0.3	

High Speed I/O (HSIO) Lane Multiplexing in KBL U PCH-LP

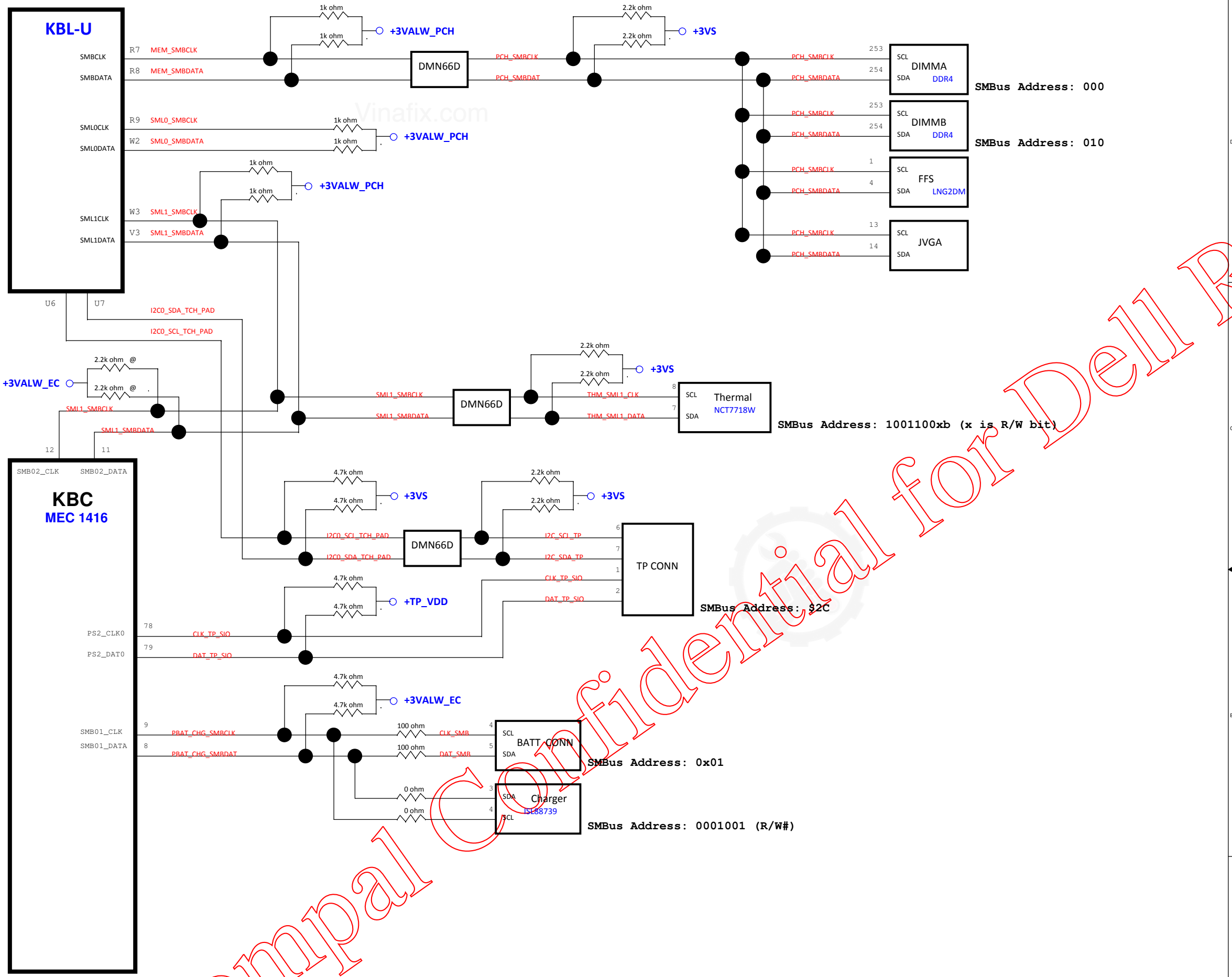


CPU PWR
Peripheral Device PWR



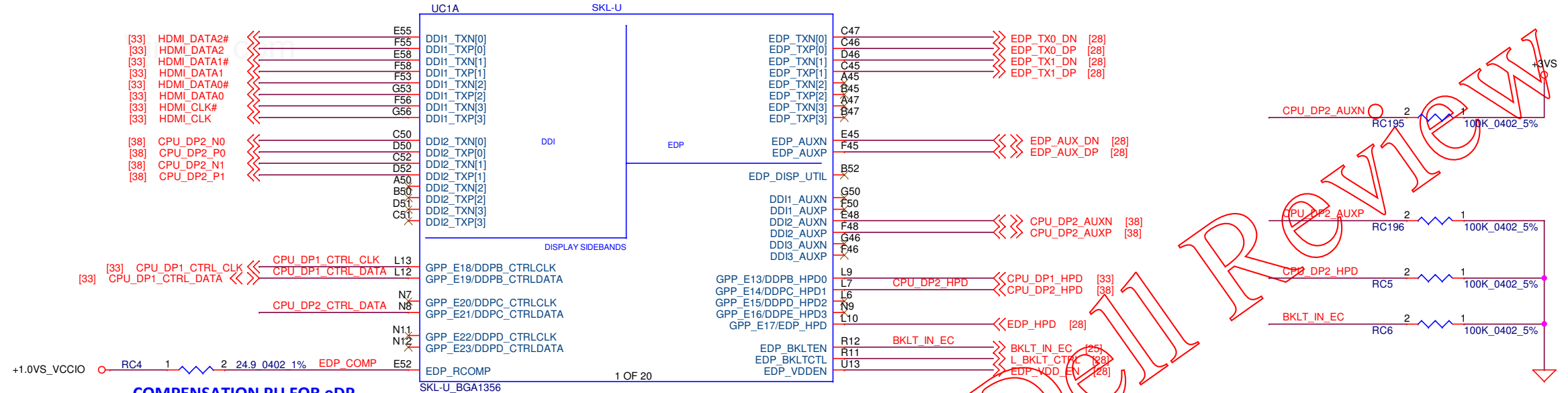
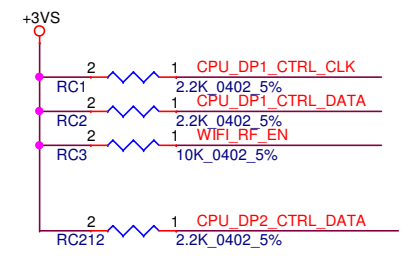
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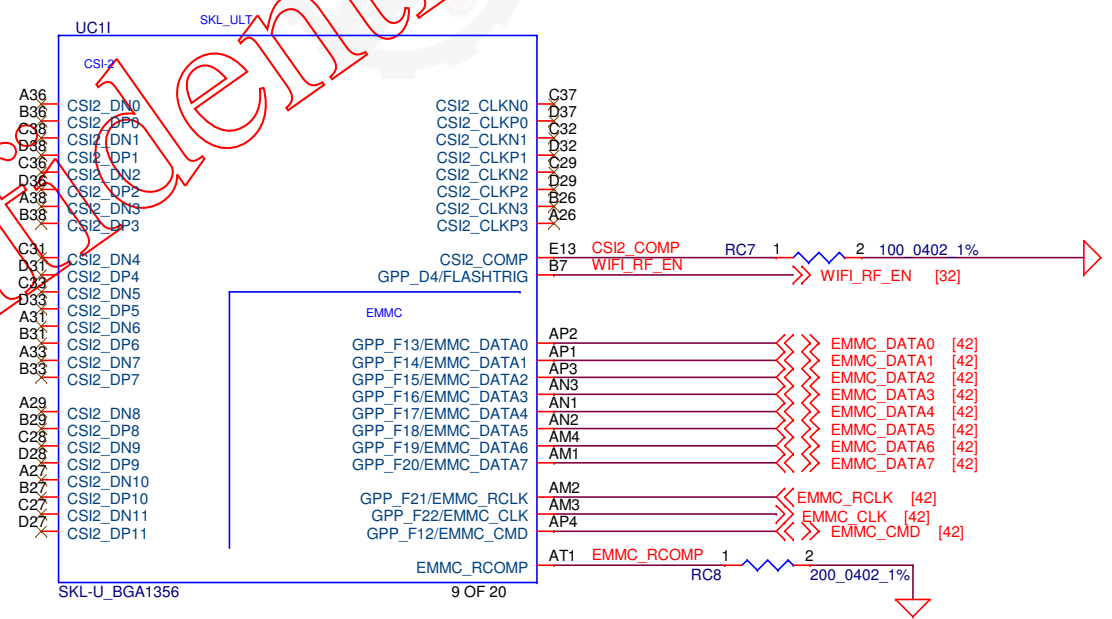


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Title	SMBus Block Diagram			
Size	Document Number	Rev		
Custom	LA-F114P	A00		
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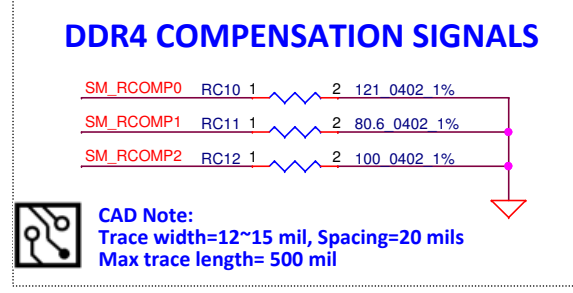
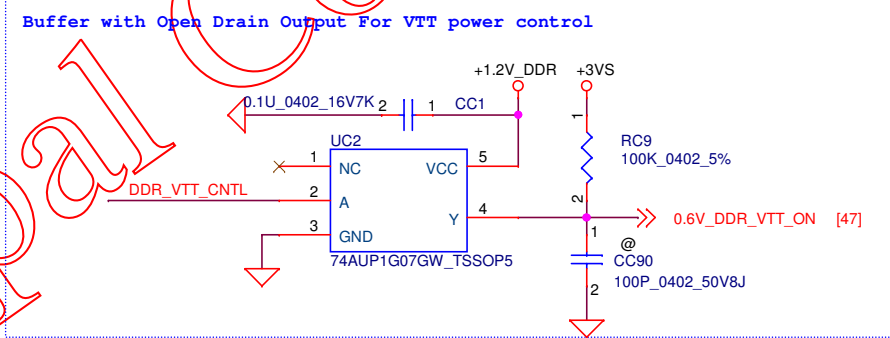
COMPENSATION PU FOR eDP
 CAD Note: Min trace width=20 mils, Spacing=25mil, Max length=100 mils. **SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0**



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DDR4 Interleaved Memory

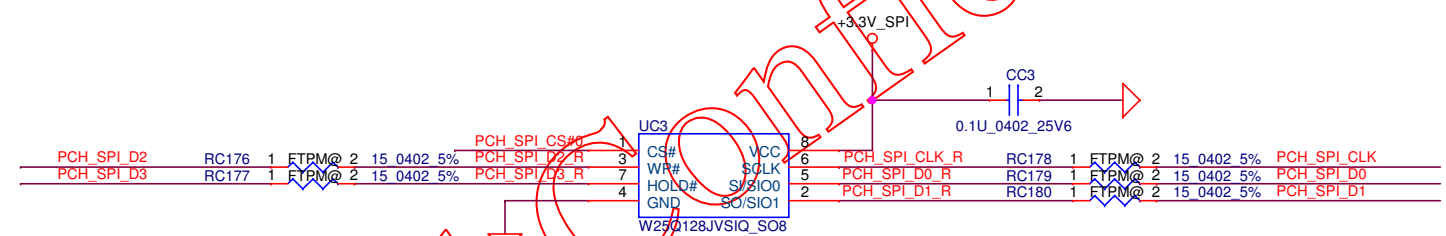
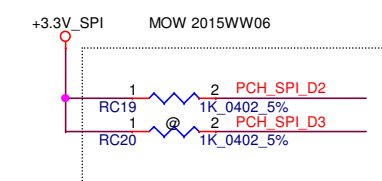
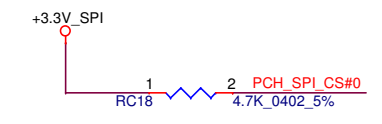
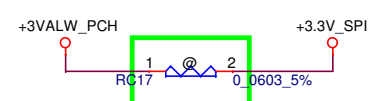
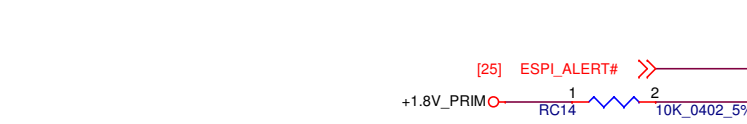
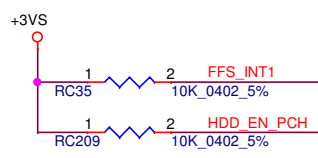


CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

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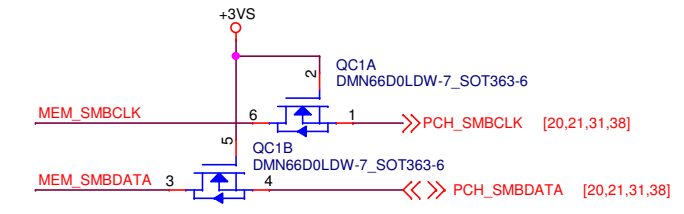
SPI_MOSI= SPI_IO0
 SPI_MISO= SPI_IO1
 PCH EDS R0.7 p.235~236



128Mb Flash ROM
UC3 place colse to UX1

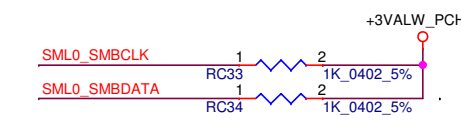
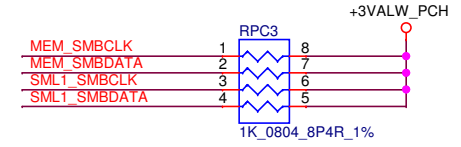
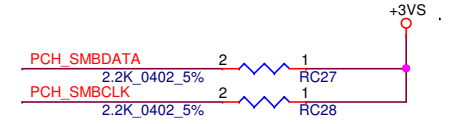
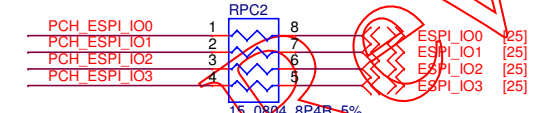
- RC176 TPM@ 33_0402_5% SD028330A80
- RC177 TPM@ 33_0402_5% SD028330A80
- RC178 TPM@ 33_0402_5% SD028330A80
- RC179 TPM@ 33_0402_5% SD028330A80
- RC180 TPM@ 33_0402_5% SD028330A80

[14] XDP_SPI_S1>> RC40 1 CMC@ 2 1K_0402_1% PCH_SPI_D0
 [14] XDP_SPI_IO2>> RC41 1 CMC@ 2 1K_0402_1% PCH_SPI_D2
 RC40/41 place to within 1100 mil of SPIO_MOSI/SPIO_IO2 pin for XDP



SMB -> DDR4, FFS

SML1 -> EC, THM



Int. PD. +3VALW_PCH

SMB_ALERT# RC37 1 @ 2 2.2K_0402_5%

TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Int. PD. +3VALW_PCH

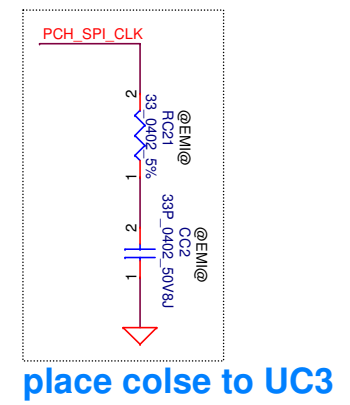
GPP_C5 RC38 1 4.7K_0402_5%

EC interface	
HIGH	ESPI
LOW(DEFAULT)	LPC

Modify Value to 150k for WW52 MOW 2015/03/03 Jason

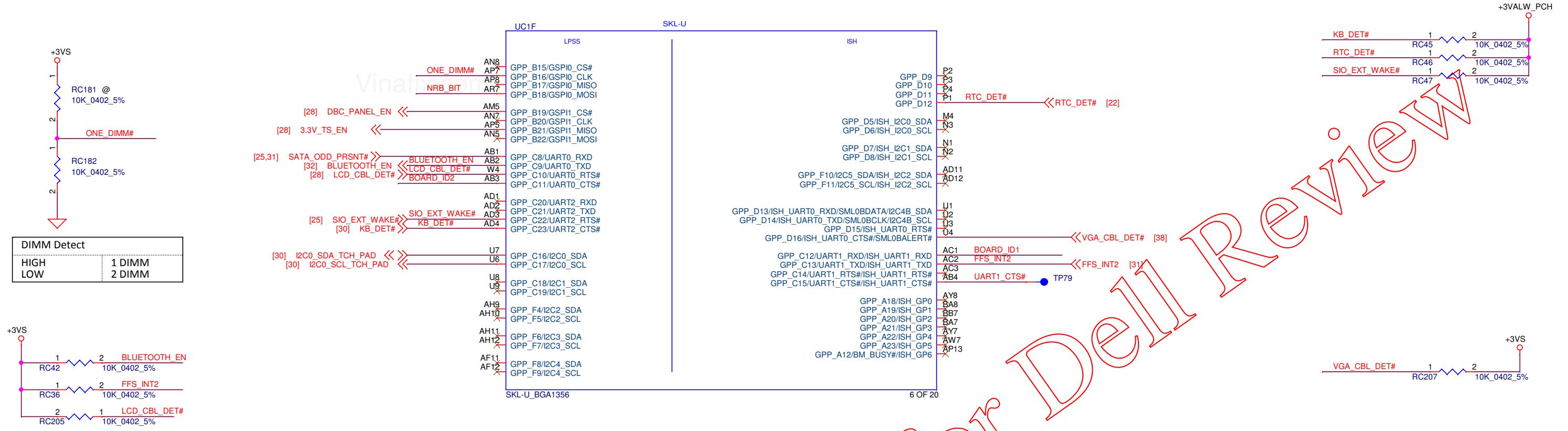
GPP_B23 RC39 1 CMC@ 2 150K_0402_5%

EXI BOOT STALL BYPASS	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE



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Main Func = CPU



DIMM Detect

HIGH	1 DIMM
LOW	2 DIMM

NO REBOOT STRAP

HIGH	No REBOOT
LOW(DEFAULT)	REBOOT ENABLE

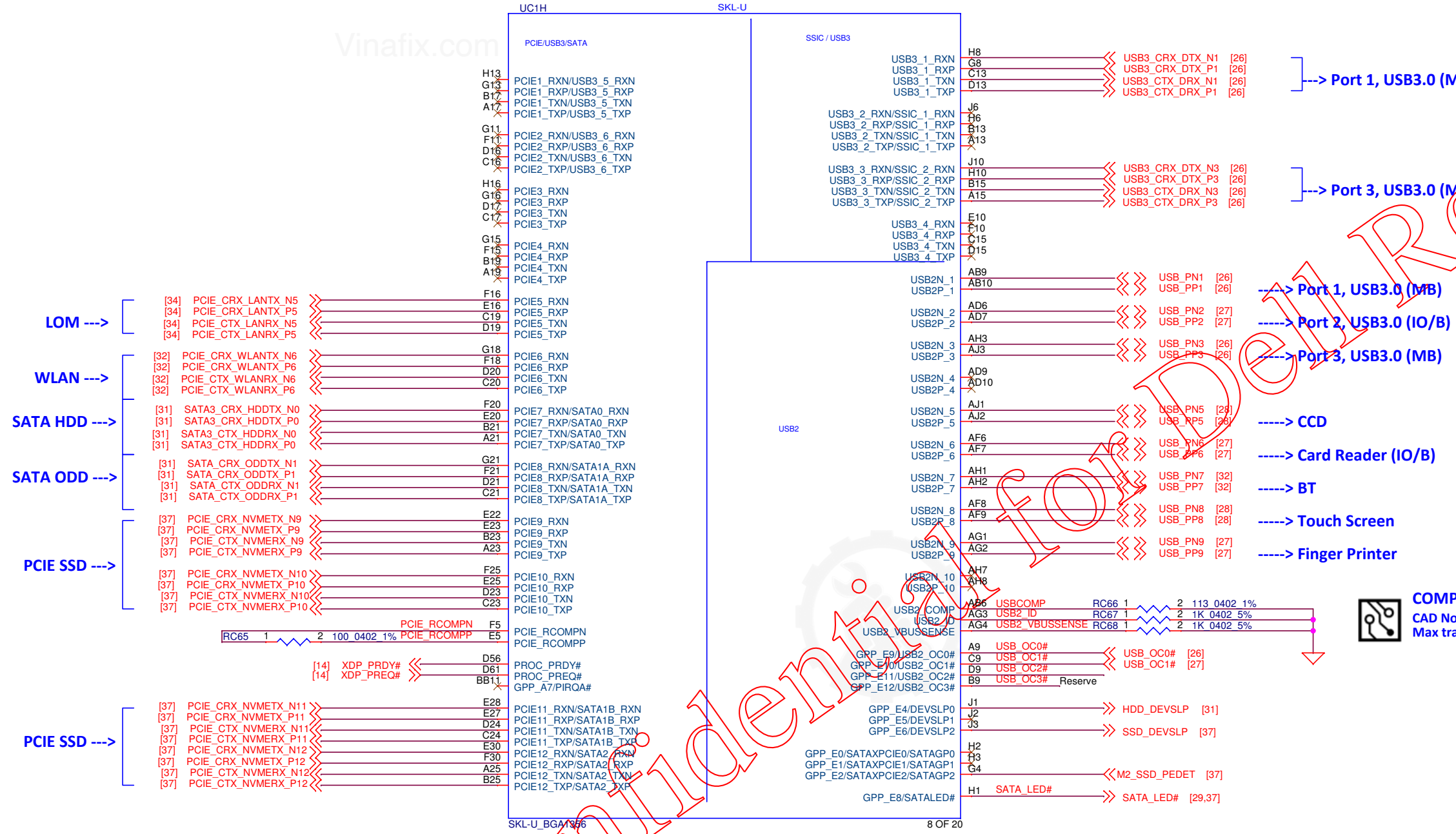
Weak IPD

CPU ID (PCBA VRAM Size Config.)	BOARD_ID2 (GPP_C11)	BOARD_ID1 (GPP_C12)
KBL-U	1	1
KBL-R	1	0
Reserved	0	1
SKL-U	0	0

- RC55 KBLR@ 10K_0402_5% SD028100280
- RC58 KBLR@ 10K_0402_5% SD028100280

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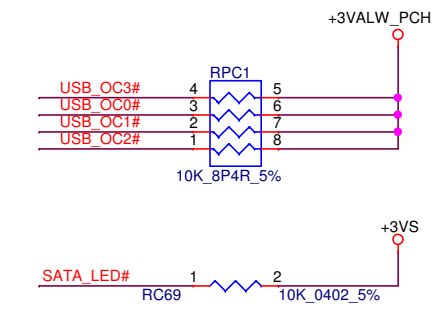


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- LOM ----> [34] PCIE_CRX_LANTX_N5
- WLAN ----> [32] PCIE_CRX_WLANTX_N6
- SATA HDD ----> [31] SATA3_CRX_HDDTX_N0
- SATA ODD ----> [31] SATA_CRX_ODDTX_N1
- PCIe SSD ----> [37] PCIE_CRX_NVMETX_N9
- PCIe SSD ----> [37] PCIE_CRX_NVMETX_N10
- PCIe SSD ----> [37] PCIE_CRX_NVMETX_P11

- > Port 1, USB3.0 (MB)
- > Port 2, USB3.0 (IO/B)
- > Port 3, USB3.0 (MB)
- > CCD
- > Card Reader (IO/B)
- > BT
- > Touch Screen
- > Finger Printer

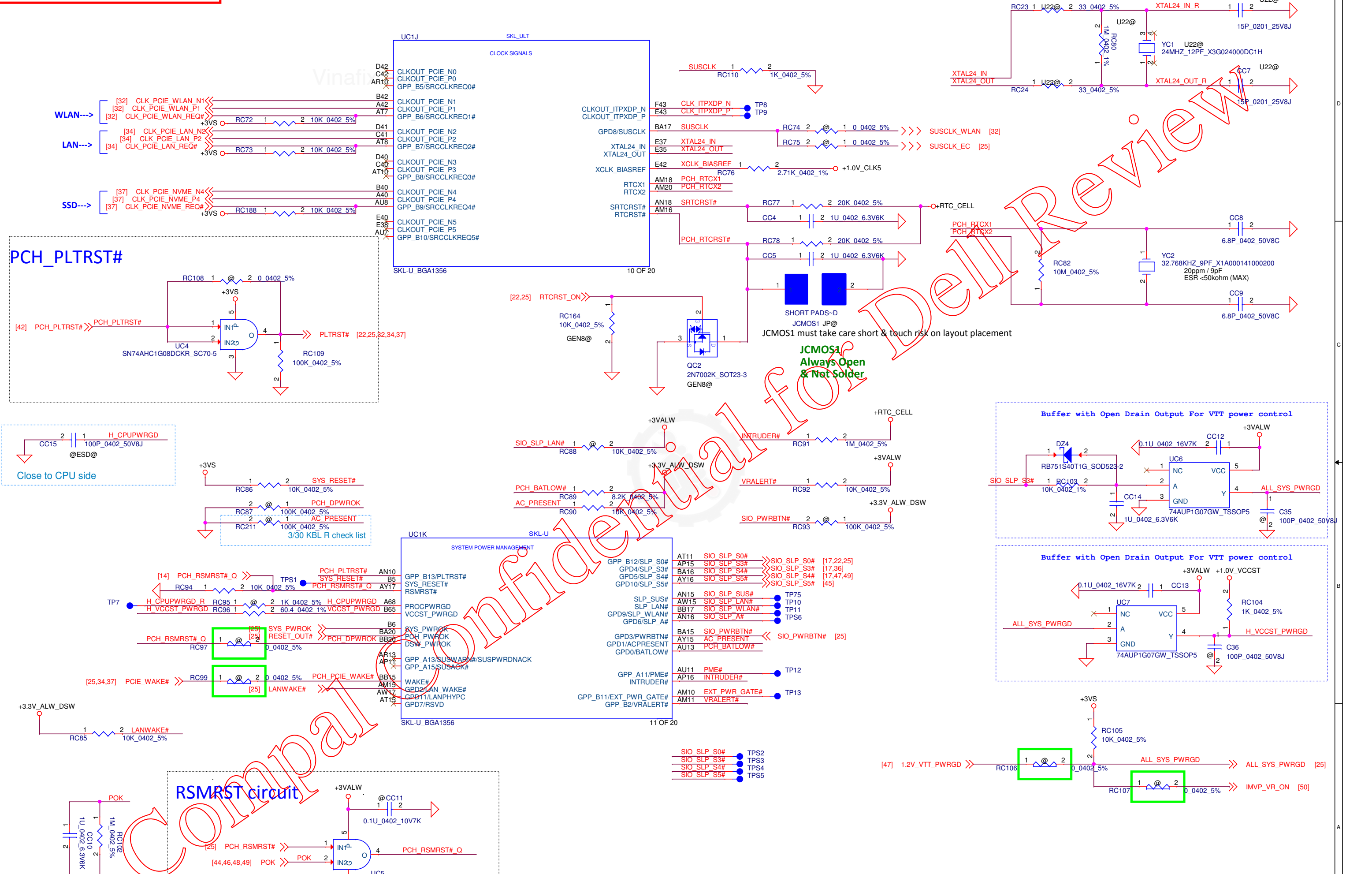
COMPENSATION PD FOR USBCOMP
 CAD Note:
 Max trace length < 1000 mil



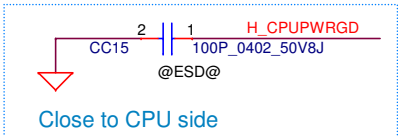
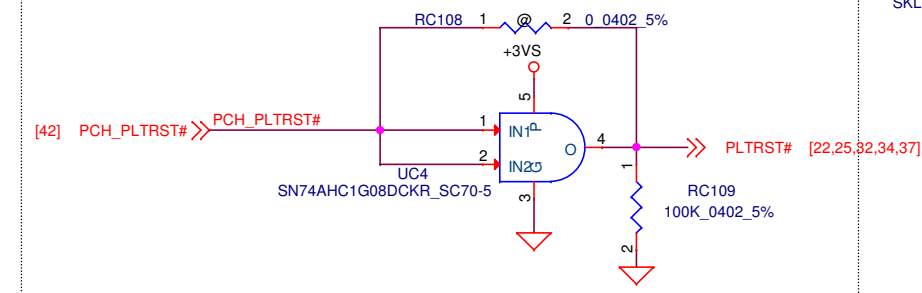
GPIO	Device Control
USB_OC0#	USB Port 1&Port3
USB_OC1#	USB Port 6
USB_OC2#	NA
USB_OC3#	NA

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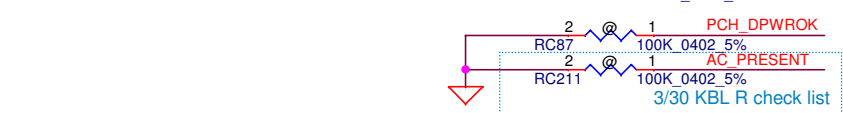
Main Func = CPU



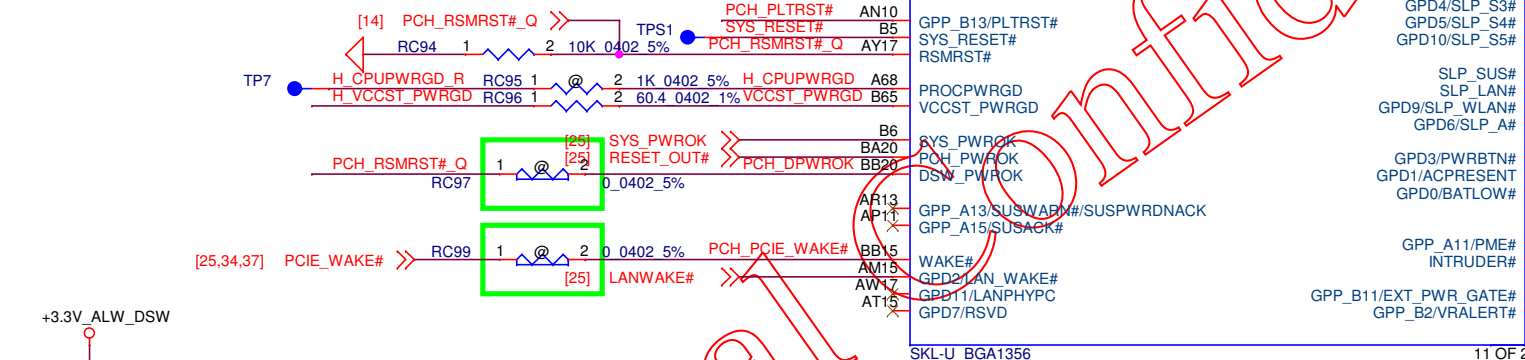
PCH_PLTRST#



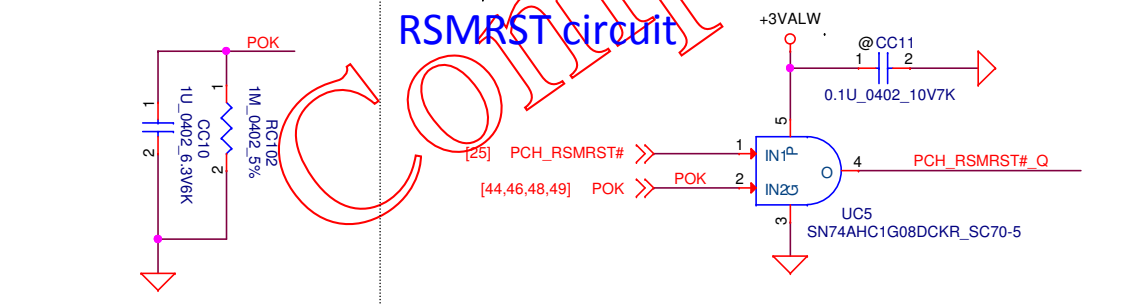
Close to CPU side



3/30 KBL R check list



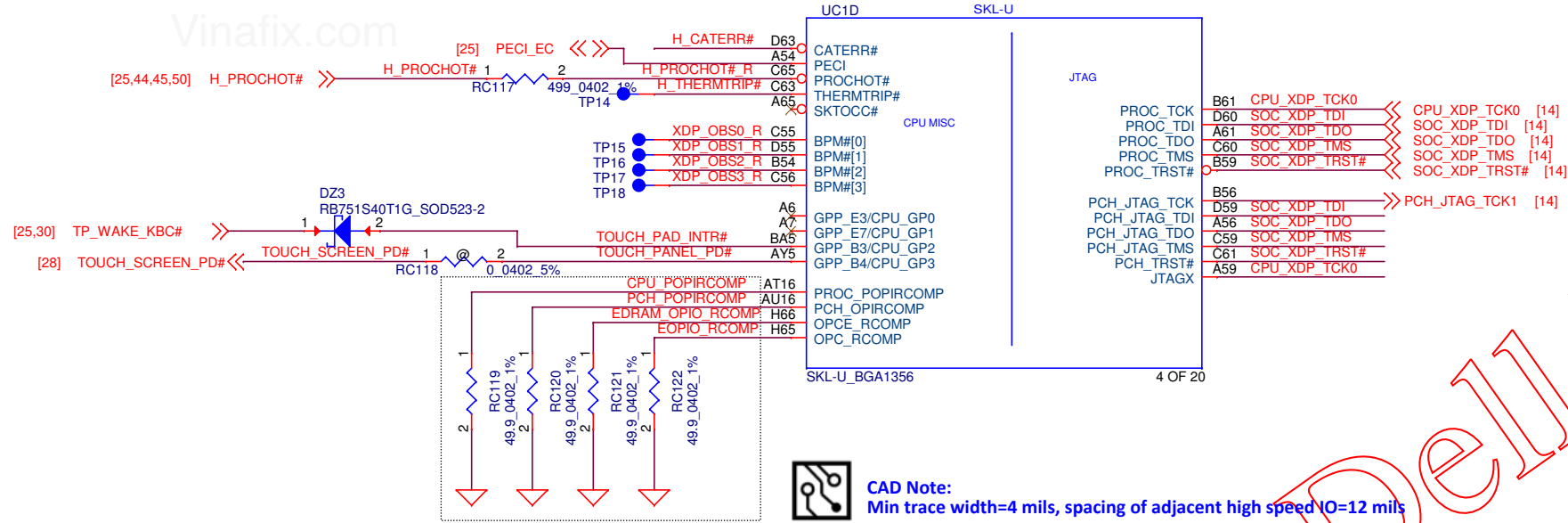
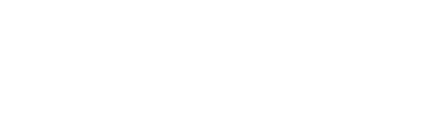
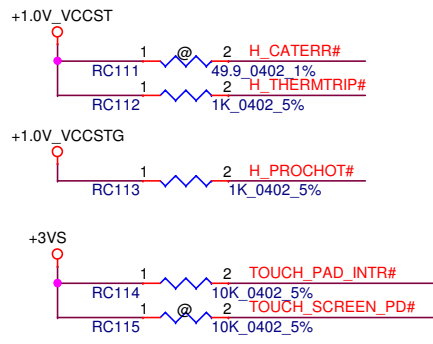
+3.3V_ALW_DSW



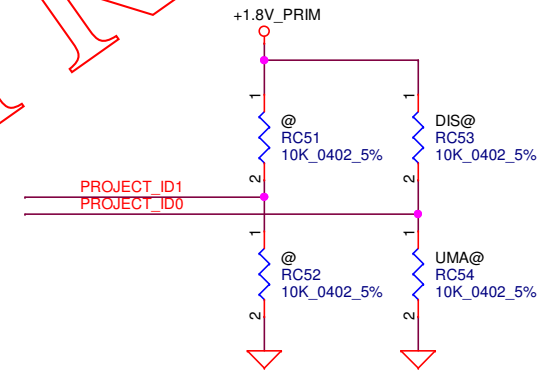
RSMRST circuit

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Main Func = CPU

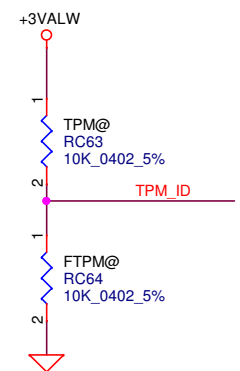
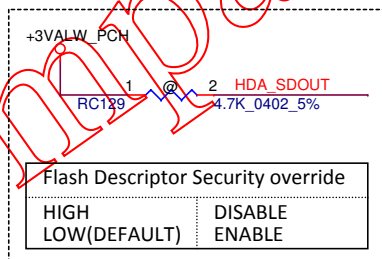
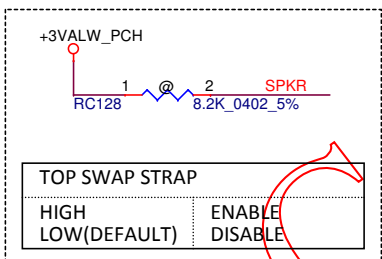
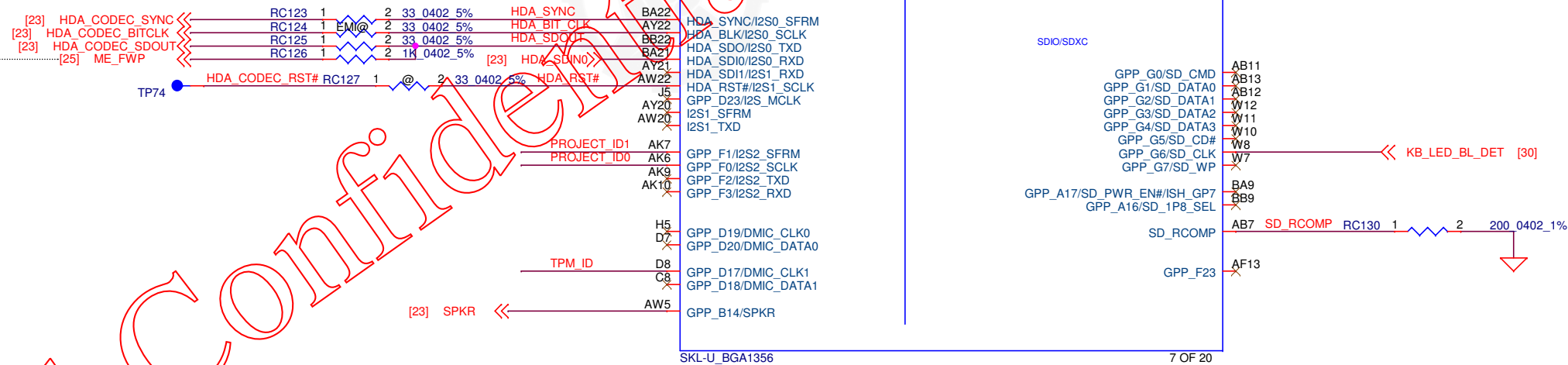
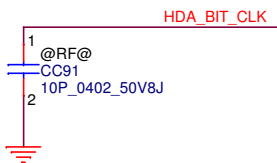


CAD Note:
Min trace width=4 mils, spacing of adjacent high speed IO=12 mils



ME_FWP

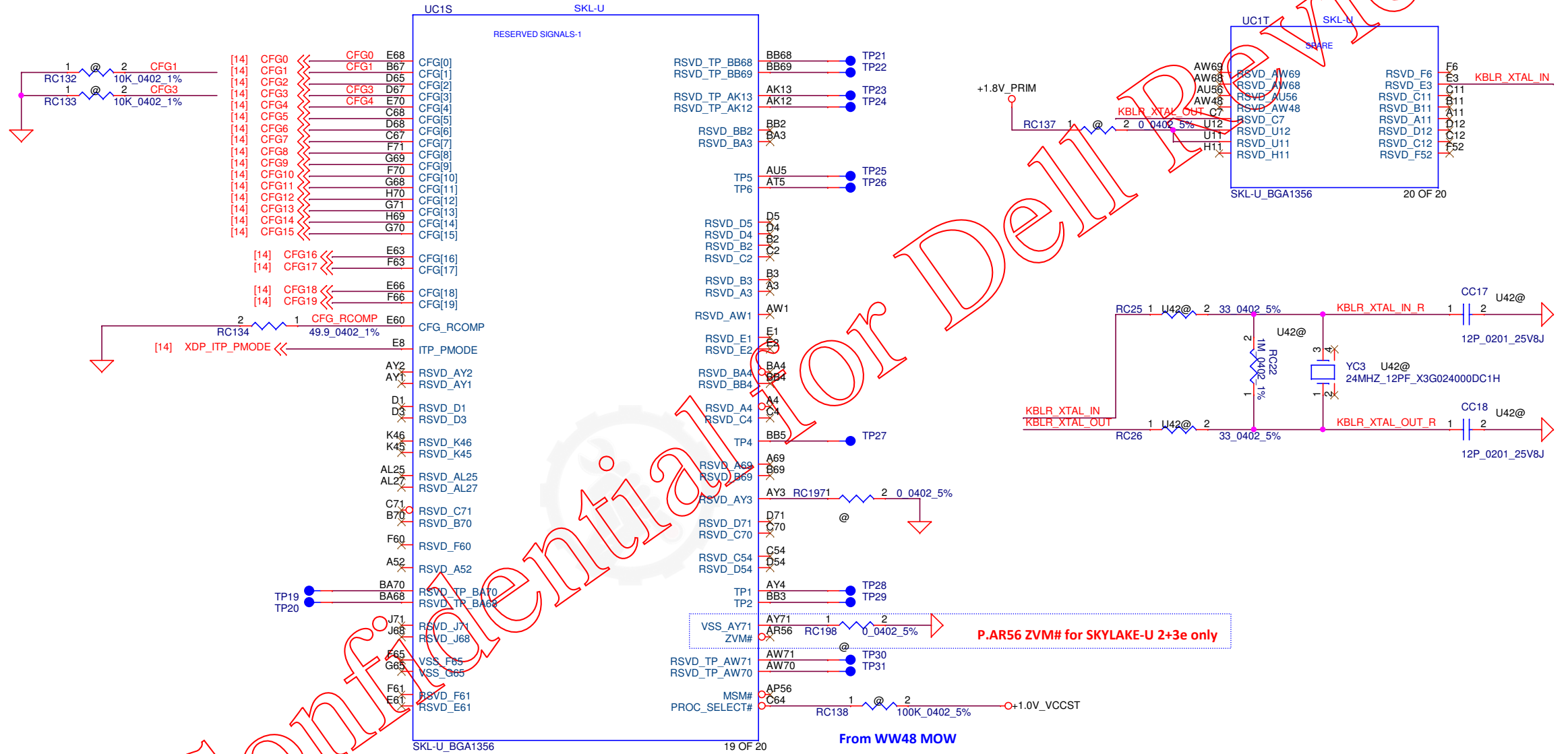
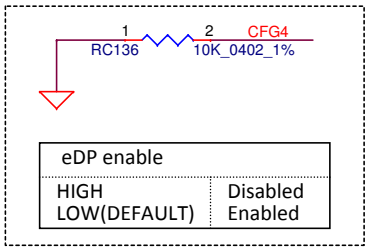
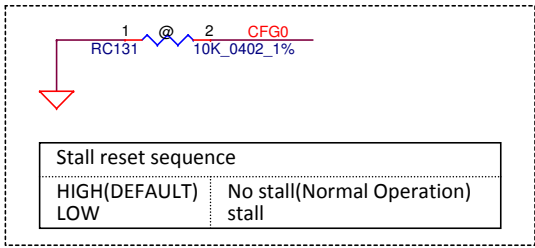
- LOW = ENABLE -->ME lock, can't update ME
- HIGH = DISABLE -->ME un-lock, can update ME



TOP SWAP STRAP	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Flash Descriptor Security override	
HIGH	DISABLE
LOW(DEFAULT)	ENABLE

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P.AR56 ZVM# for SKYLAKE-U 2+3e only

From WW48 MOW
 Stuff 100k(RC138) for Cannonlake
 Un-stuff 100k(RC138) for Skylake

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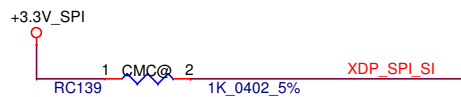
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Connector Less Routing Topology

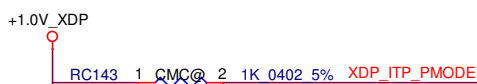
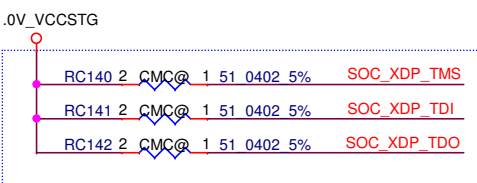
Vinafix.com

PRIMARY CMC CONN

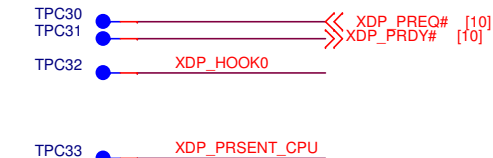
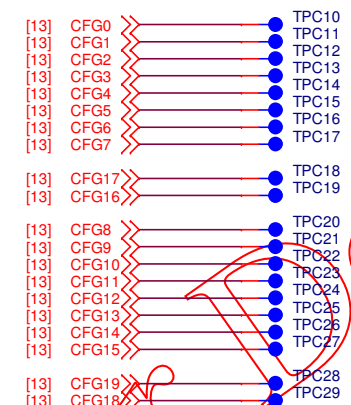
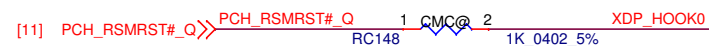
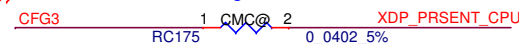
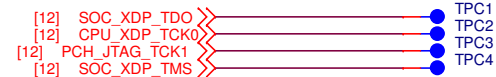
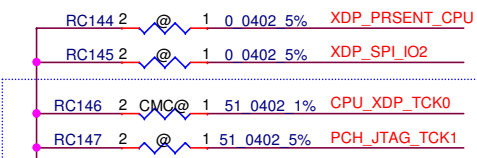
DCI Link
RC142 need POP
RC146 need POP



Place to CPU side



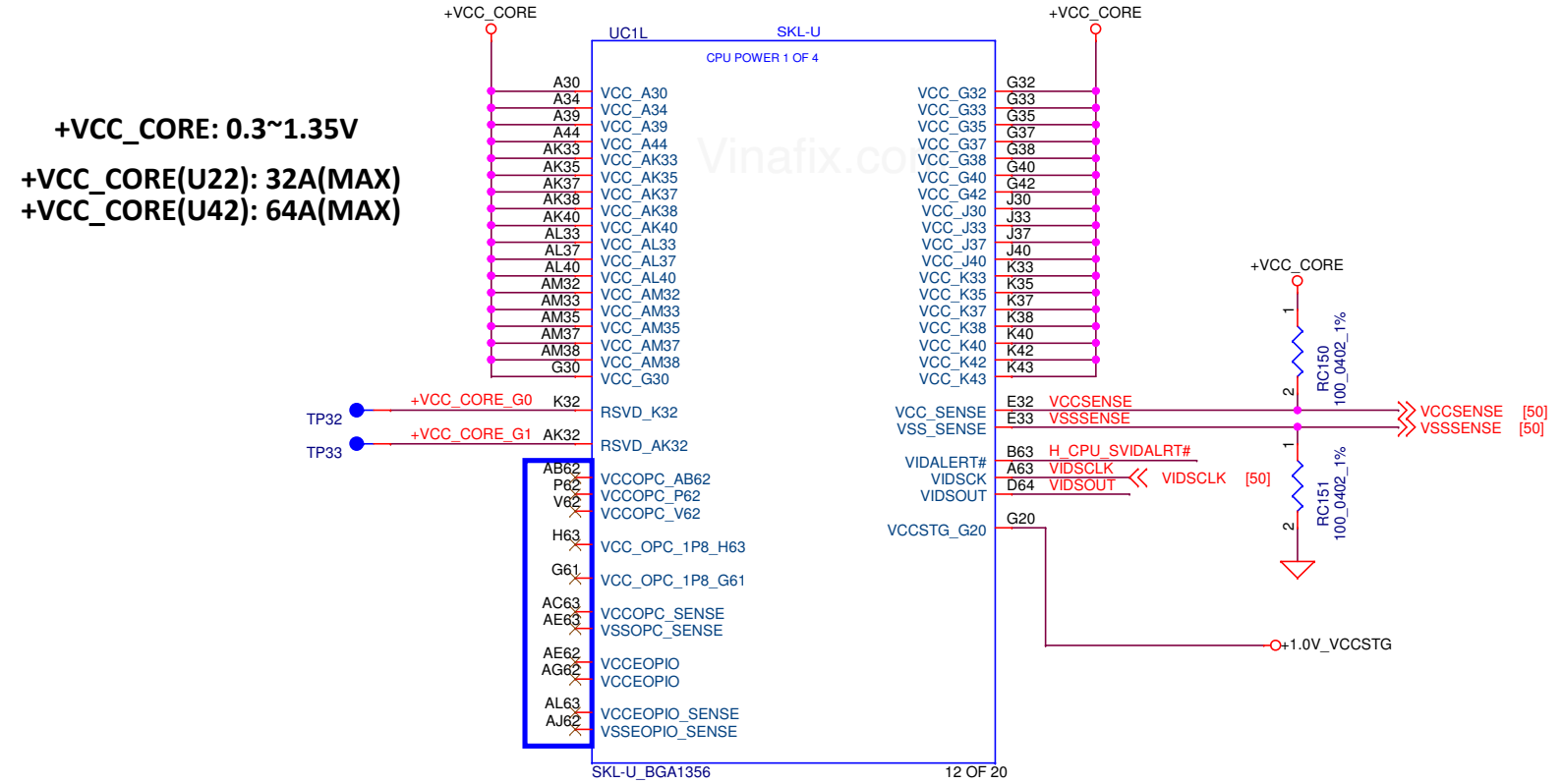
Place to CPU side



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Main Func = CPU

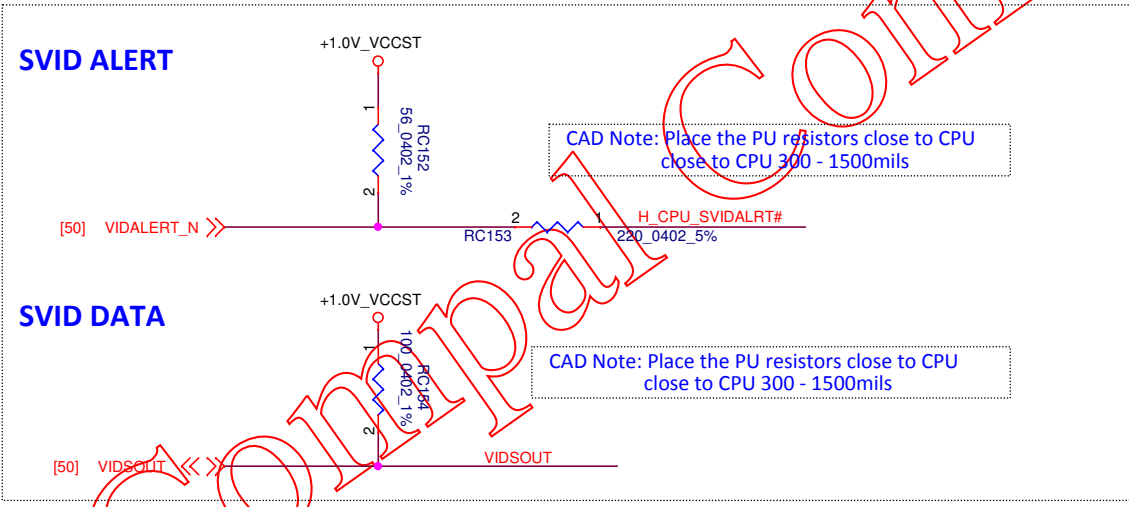


+VCC_CORE: 0.3~1.35V
+VCC_CORE(U22): 32A(MAX)
+VCC_CORE(U42): 64A(MAX)

PSC(Primary side cap) : Place as close to the package as possible
 BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
 Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

VCCOPC, VCCOPC_1P8, VCCEOPIO for SKYLAKE-U 2+3e
 (w/ on package cache)

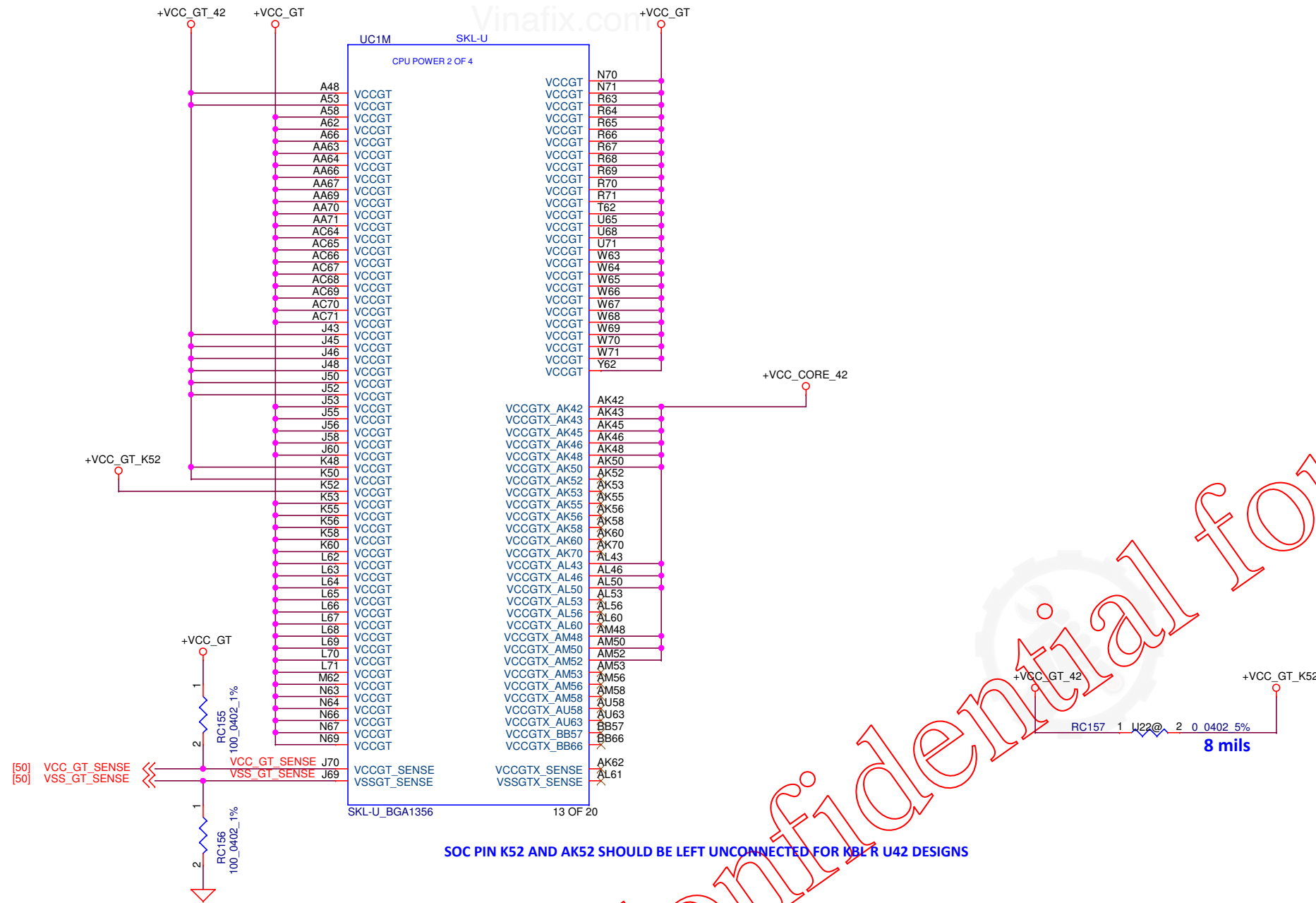


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Main Func = CPU

+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V

+VCC_GT(U22): 31A(MAX)
+VCC_GT(U42): 28A(MAX)

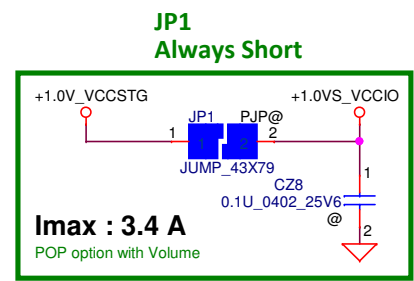
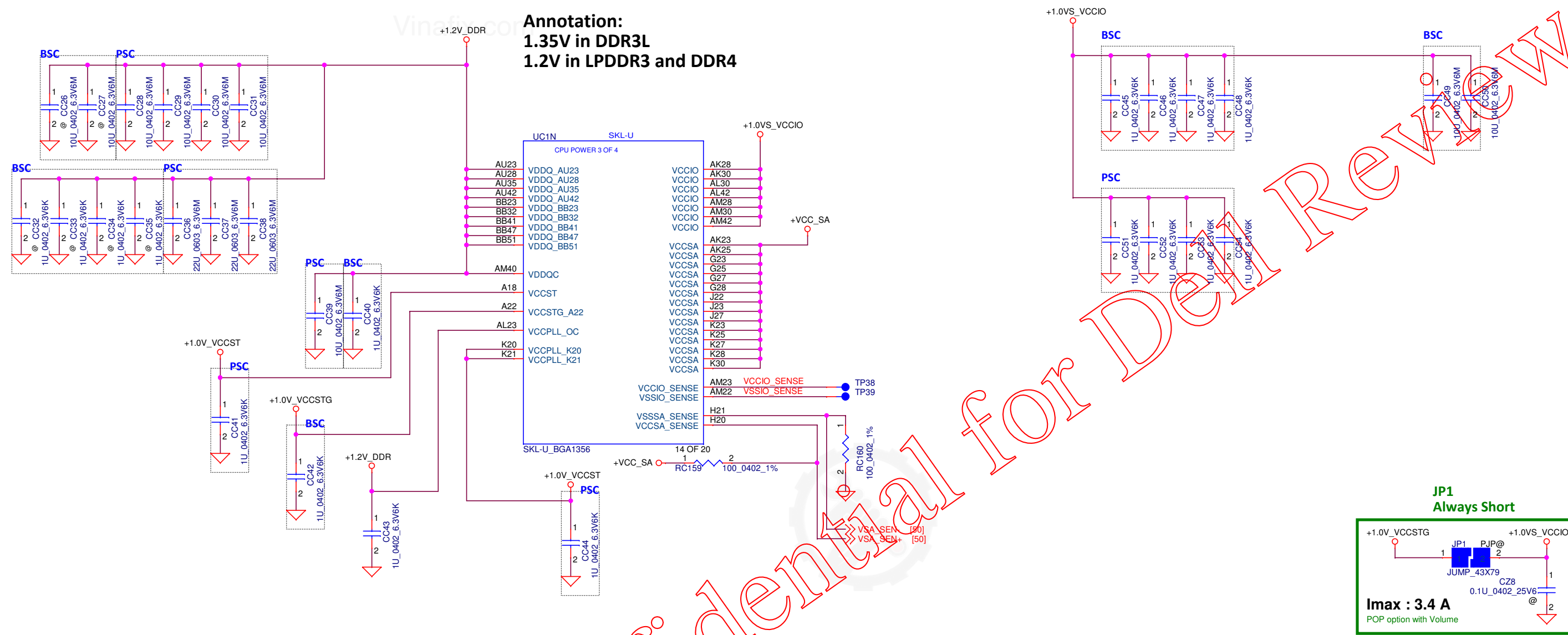


SOC PIN K52 AND AK52 SHOULD BE LEFT UNCONNECTED FOR KBL R U42 DESIGNS

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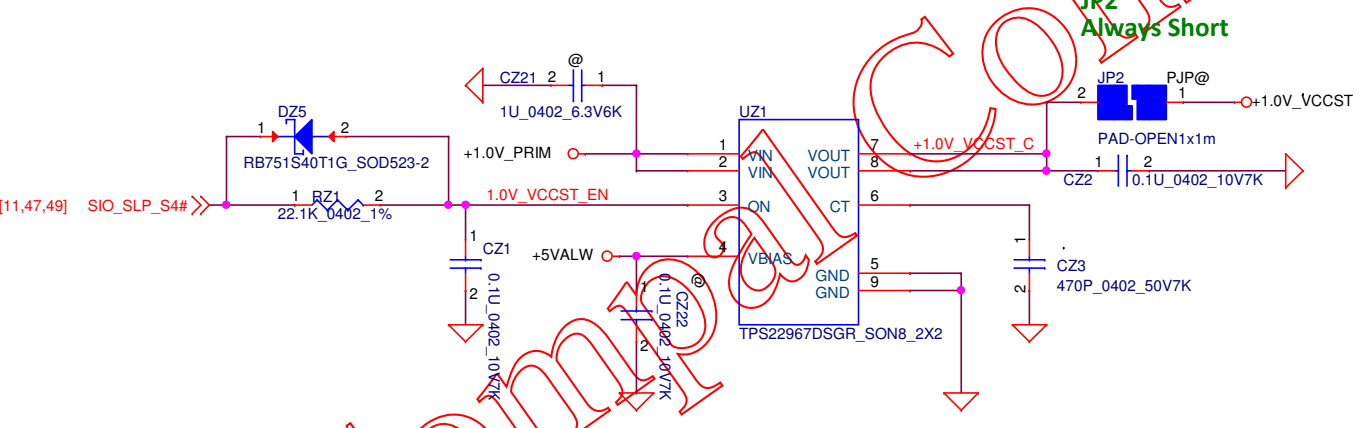
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Annotation:
1.35V in DDR3L
1.2V in LPDDR3 and DDR4



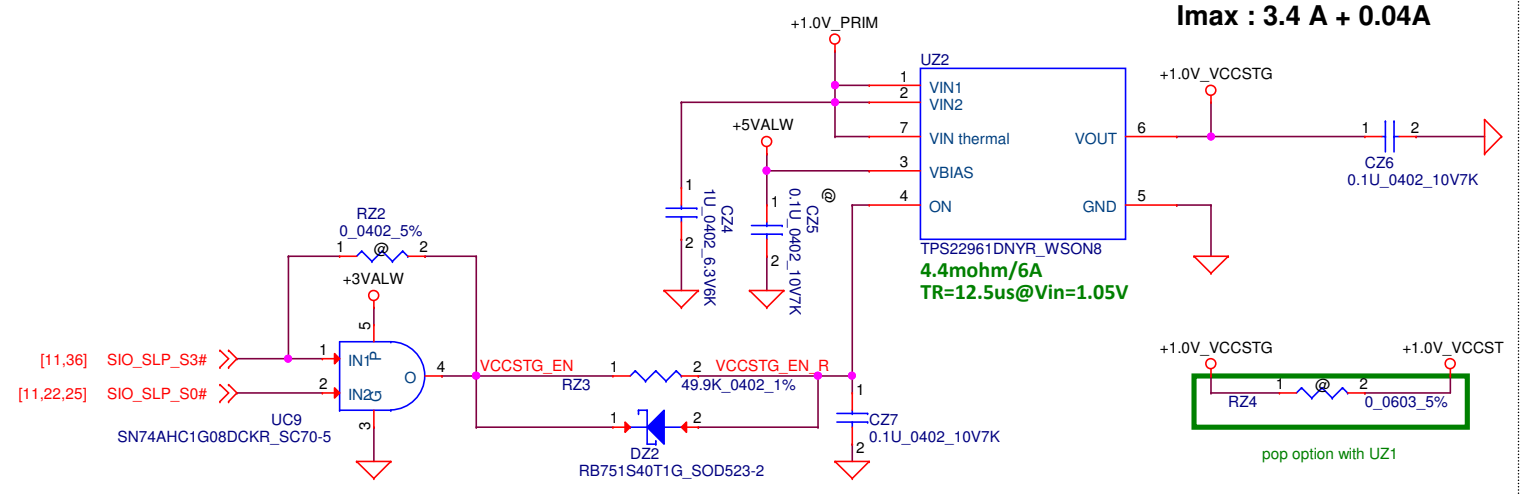
+1.0V_VCCST source

I_{max} : 0.24 A
JP2 Always Short



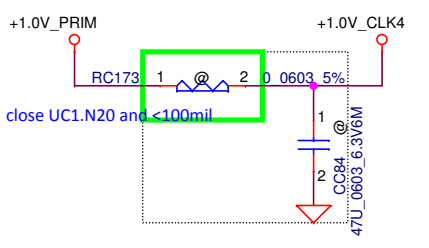
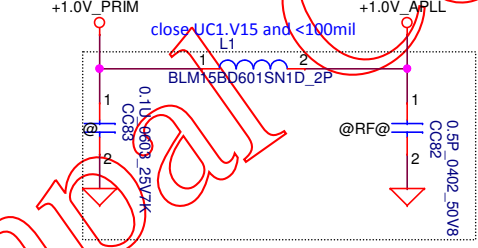
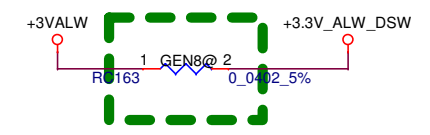
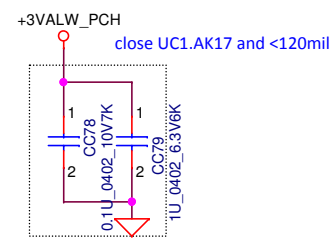
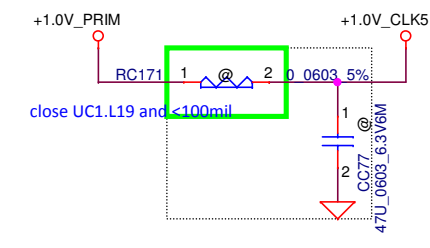
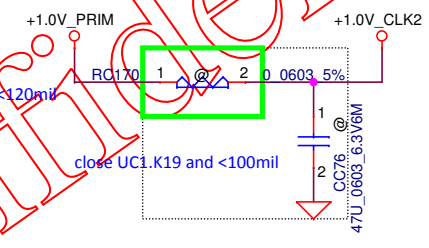
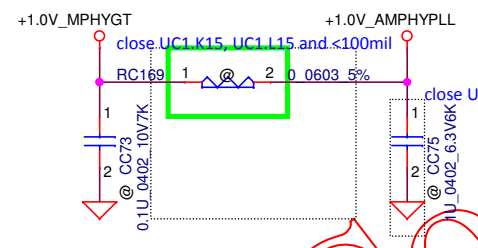
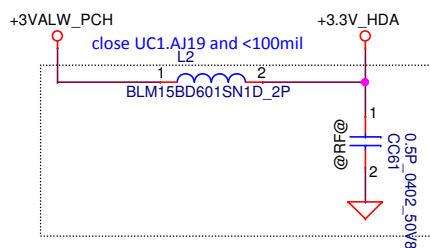
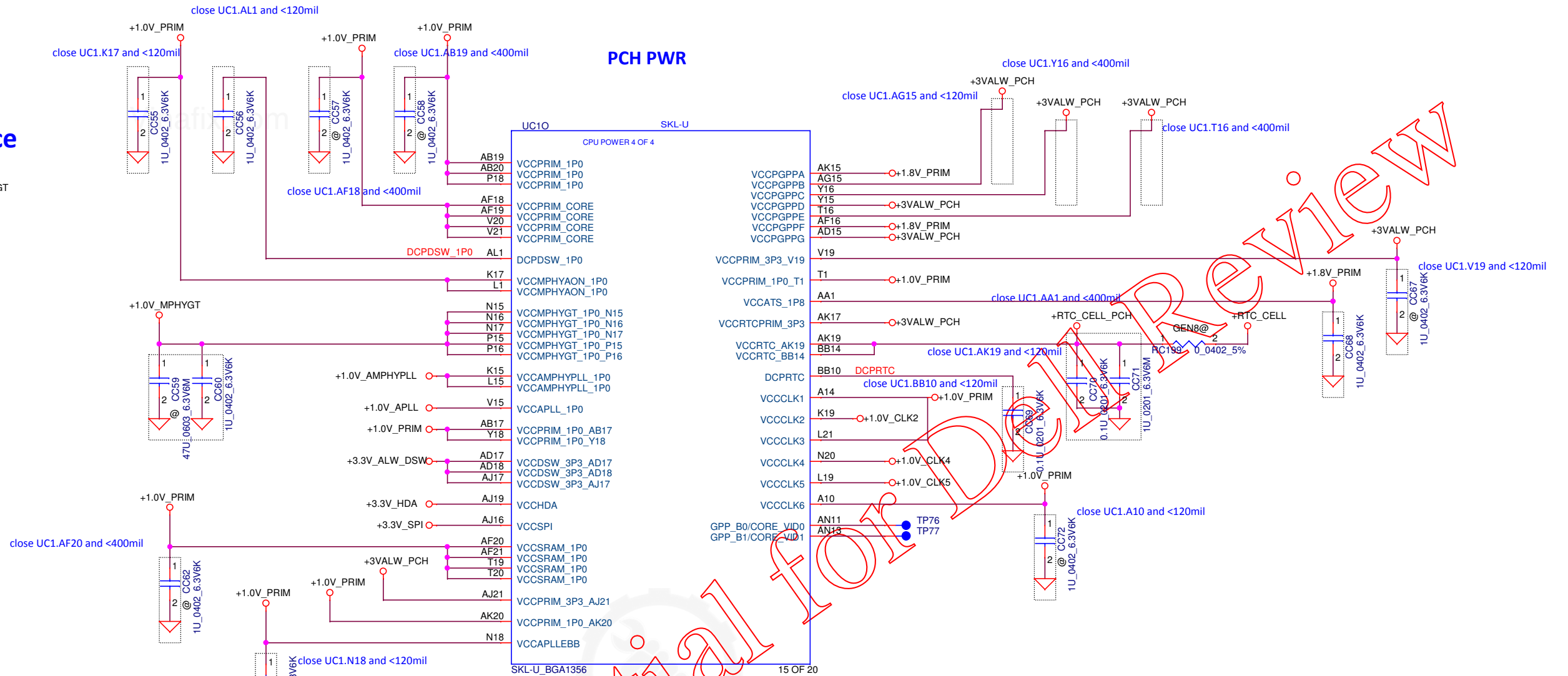
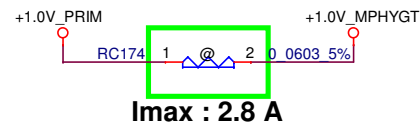
+1.0V_VCCSTG source

I_{max} : 3.4 A + 0.04A



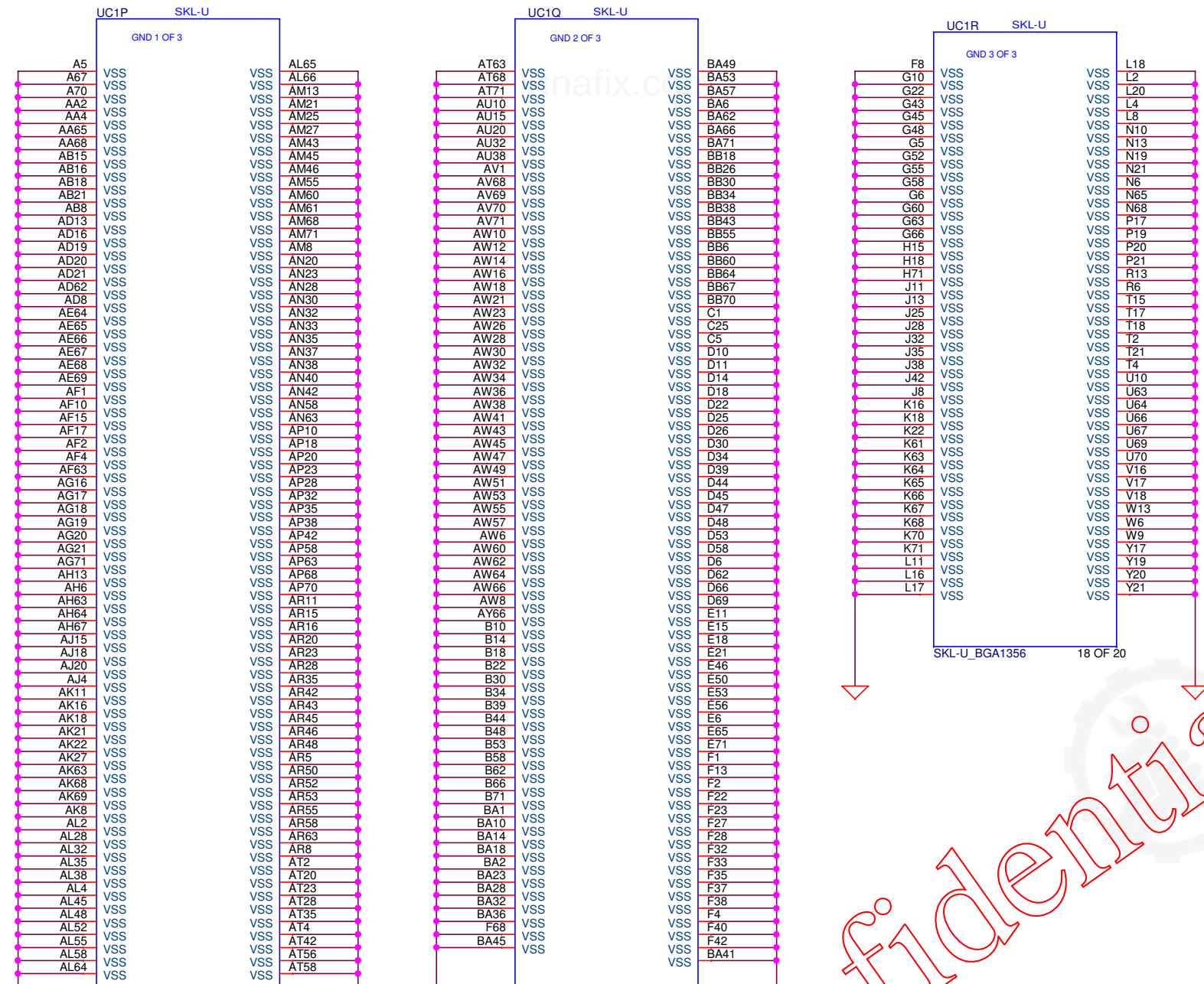
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+1.0V_MPHYGT source



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For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

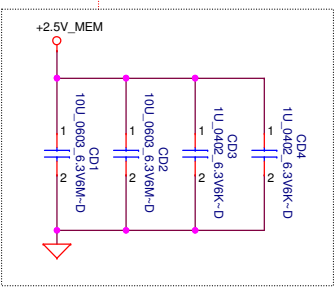
For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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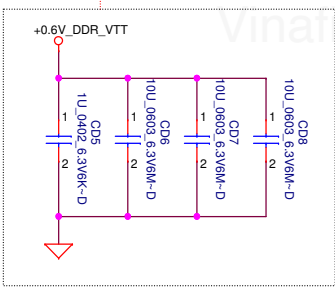
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Main Func = DDR

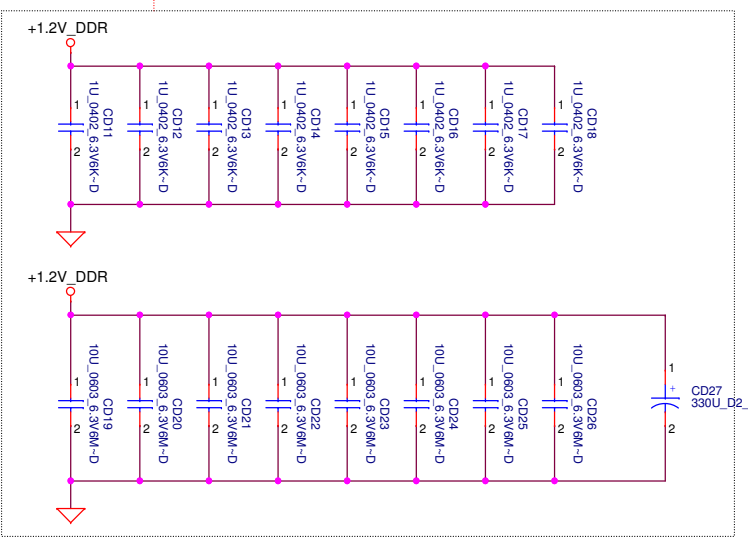
Layout Note:
Place near JDIMM1.257,259



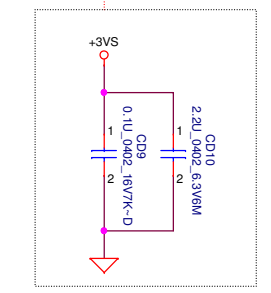
Layout Note:
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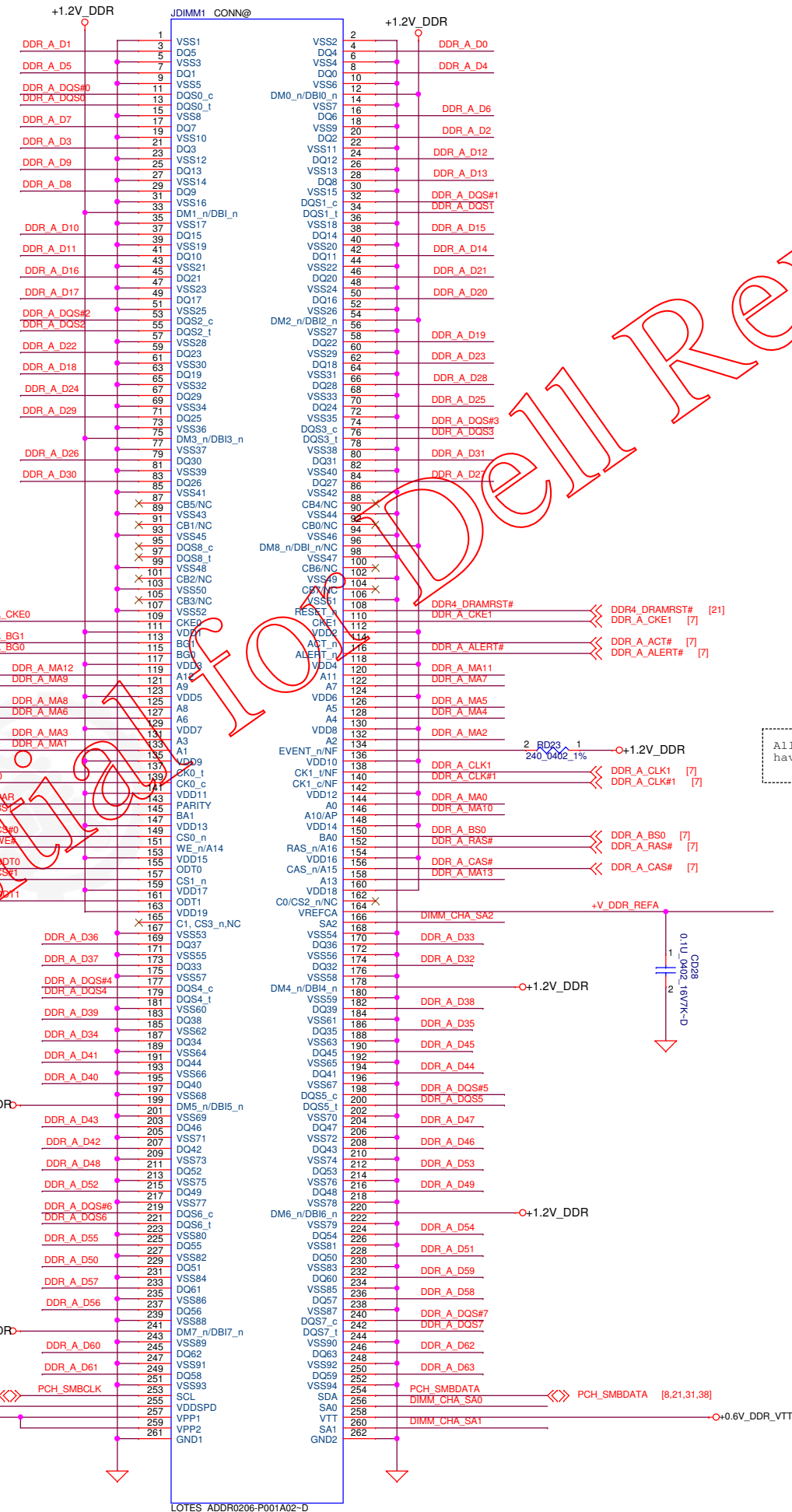
Layout Note:
Place near JDIMM1



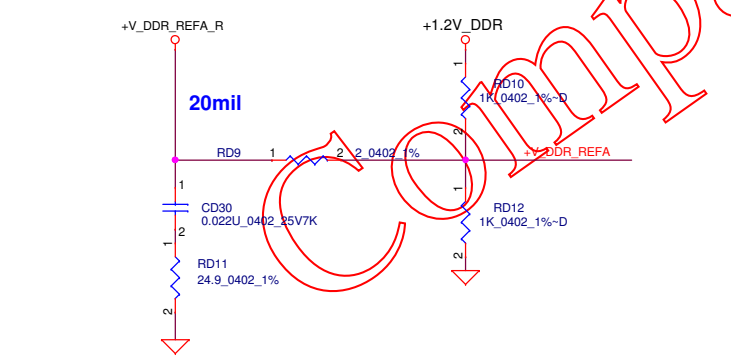
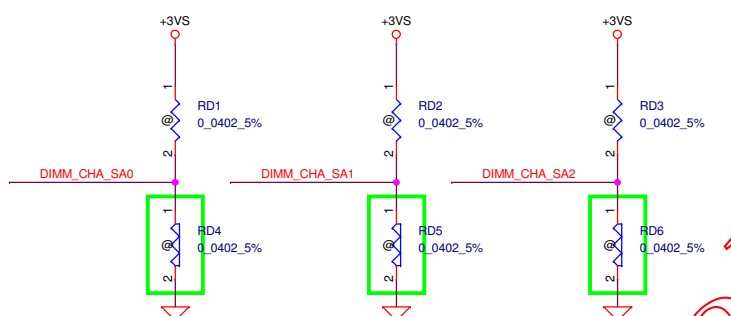
Layout Note:
Place near JDIMM1.255



- [7] DDR_A_D[0..63]
- [7] DDR_A_MA[0..13]
- [7] DDR_A_DQS[0..7]
- [7] DDR_A_DQS[0..7]



All VREF traces should have 10 mil trace width

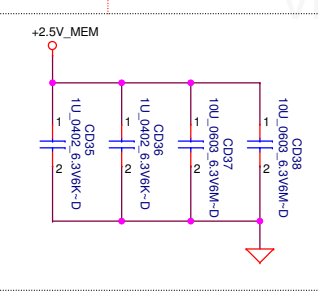
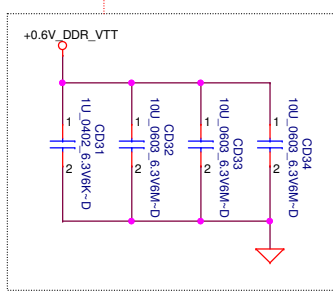


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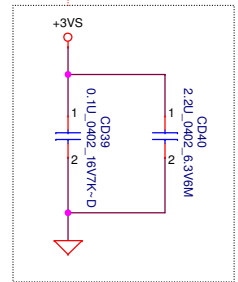
Main Func = DDR

Layout Note:
Place near JDIMM2.258

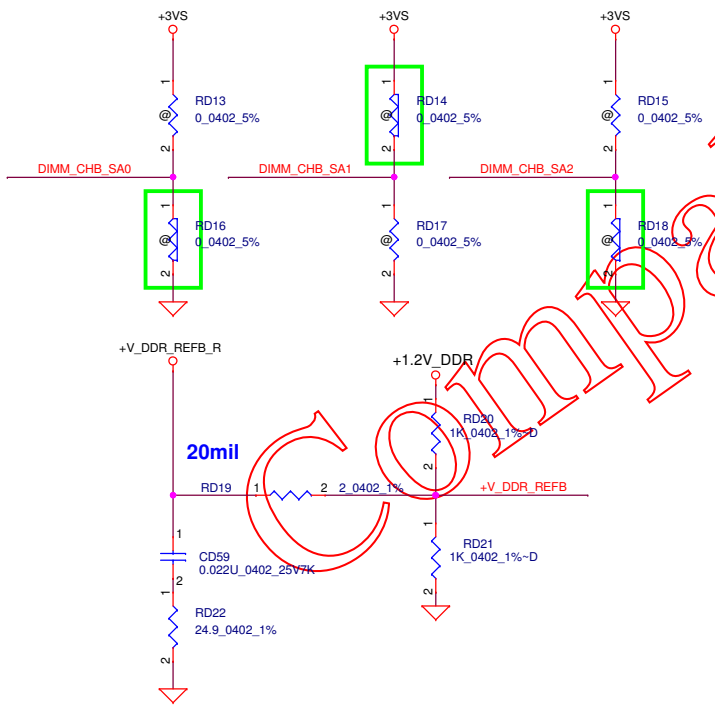
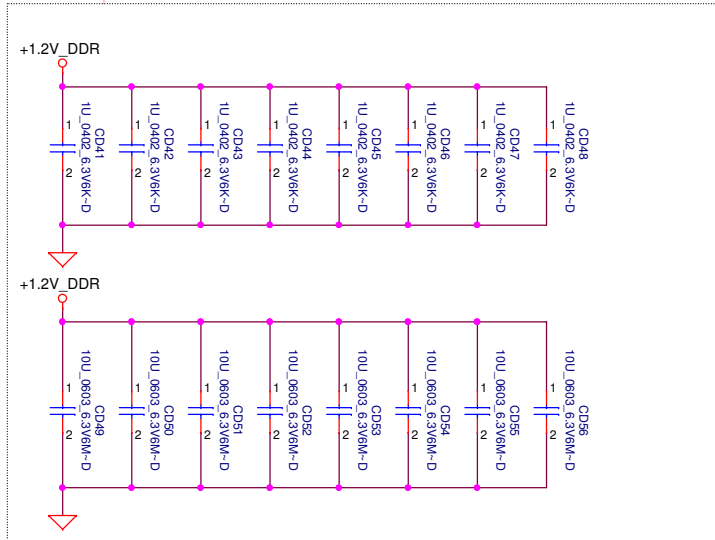
Layout Note:
Place near JDIMM2.257,259



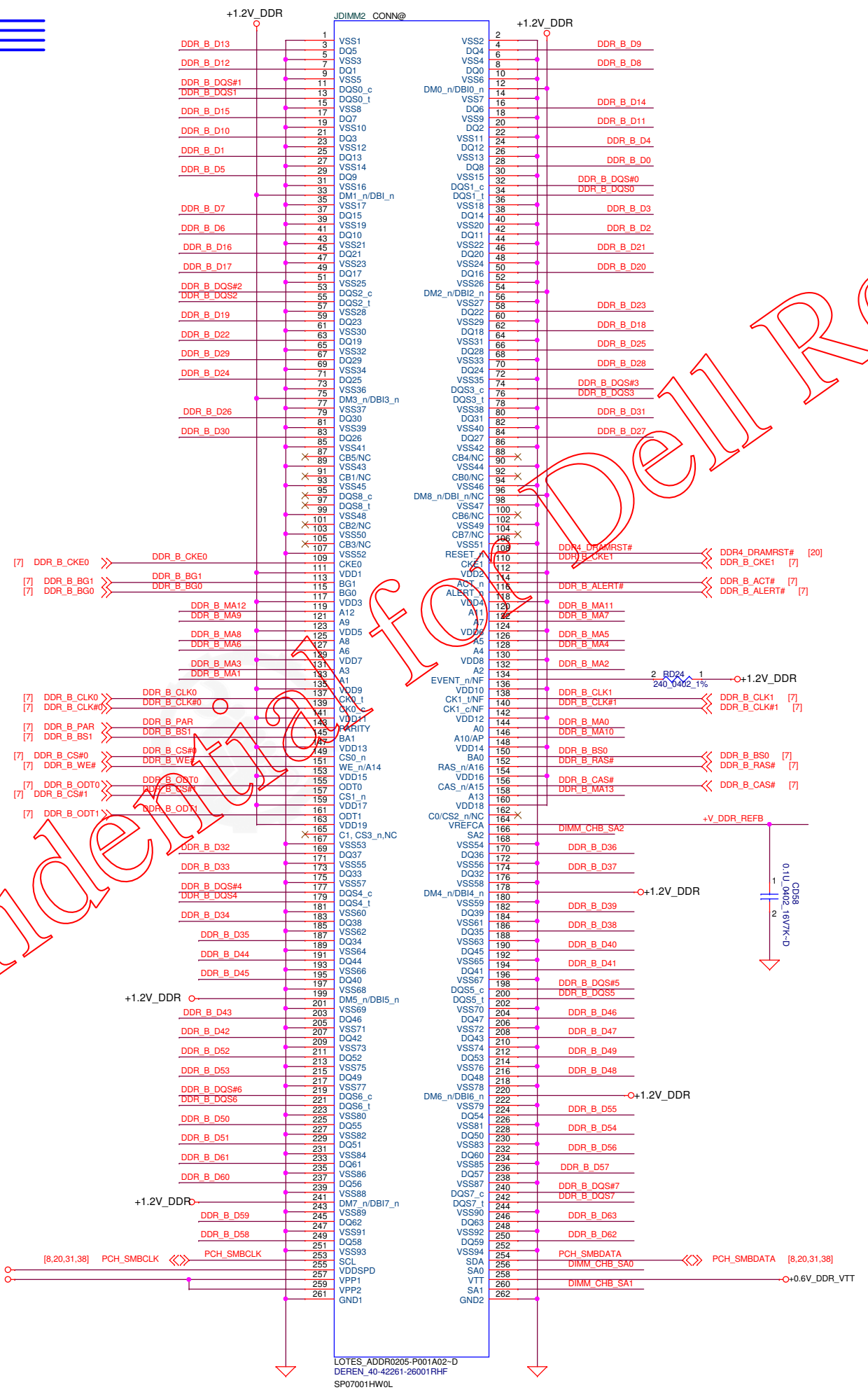
Layout Note:
Place near JDIMM2.255



Layout Note:
Place near JDIMM2



- [7] DDR_B_D[0..63]
- [7] DDR_B_MA[0..13]
- [7] DDR_B_DQS[0..7]
- [7] DDR_B_DQS[0..7]



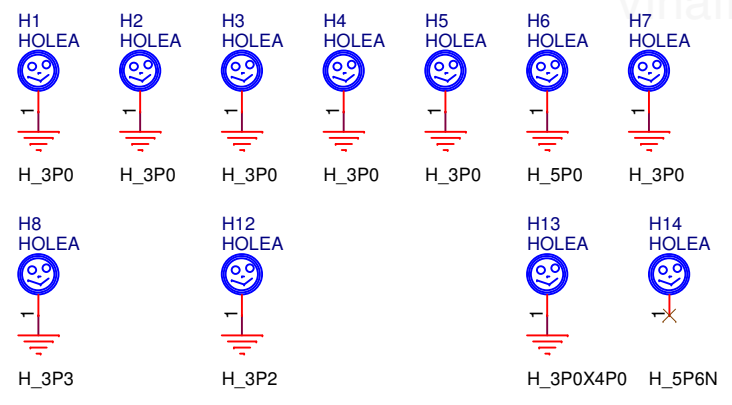
All VREF traces should have 10 mil trace width

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 for Design Review

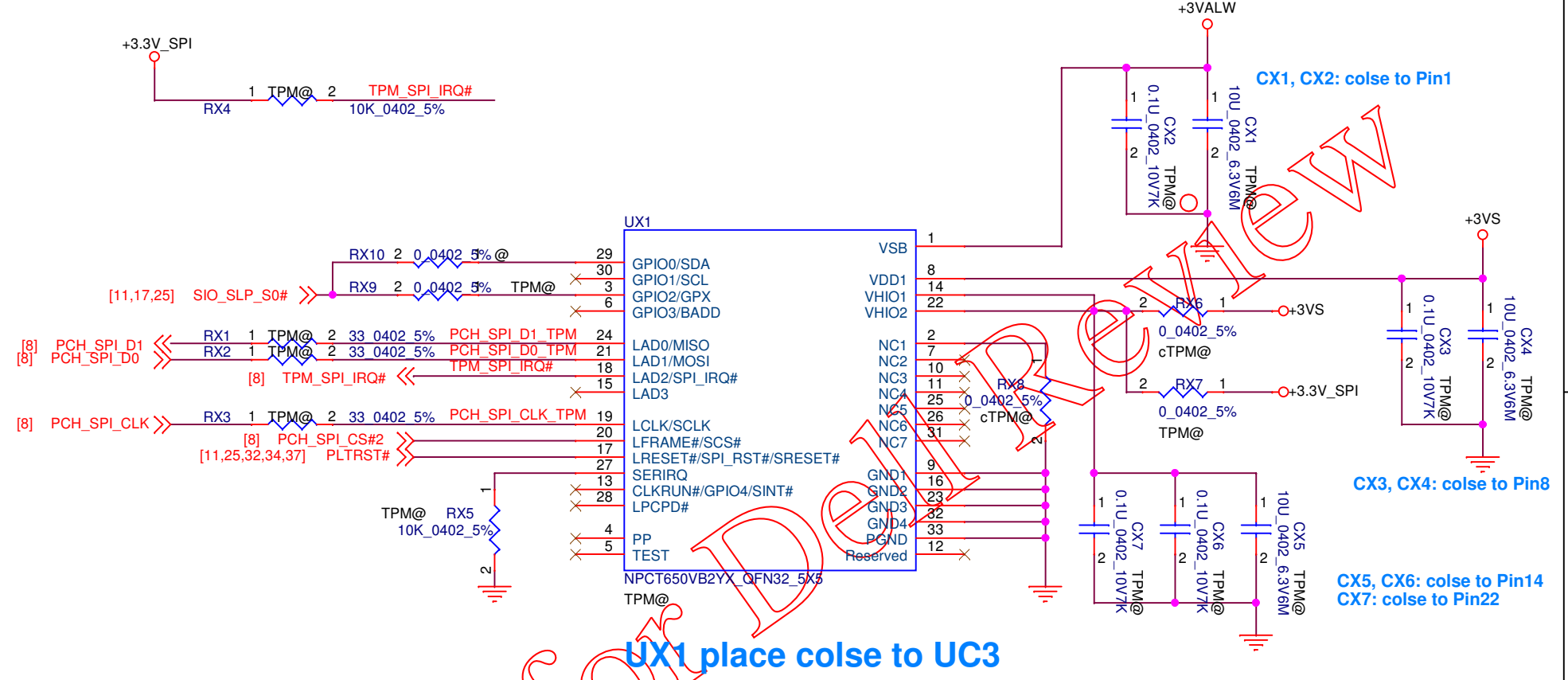
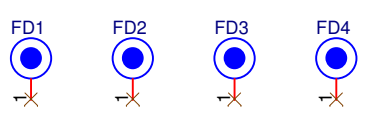
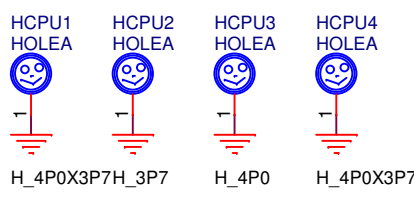
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Main Func = TPM

Screw hole/FD

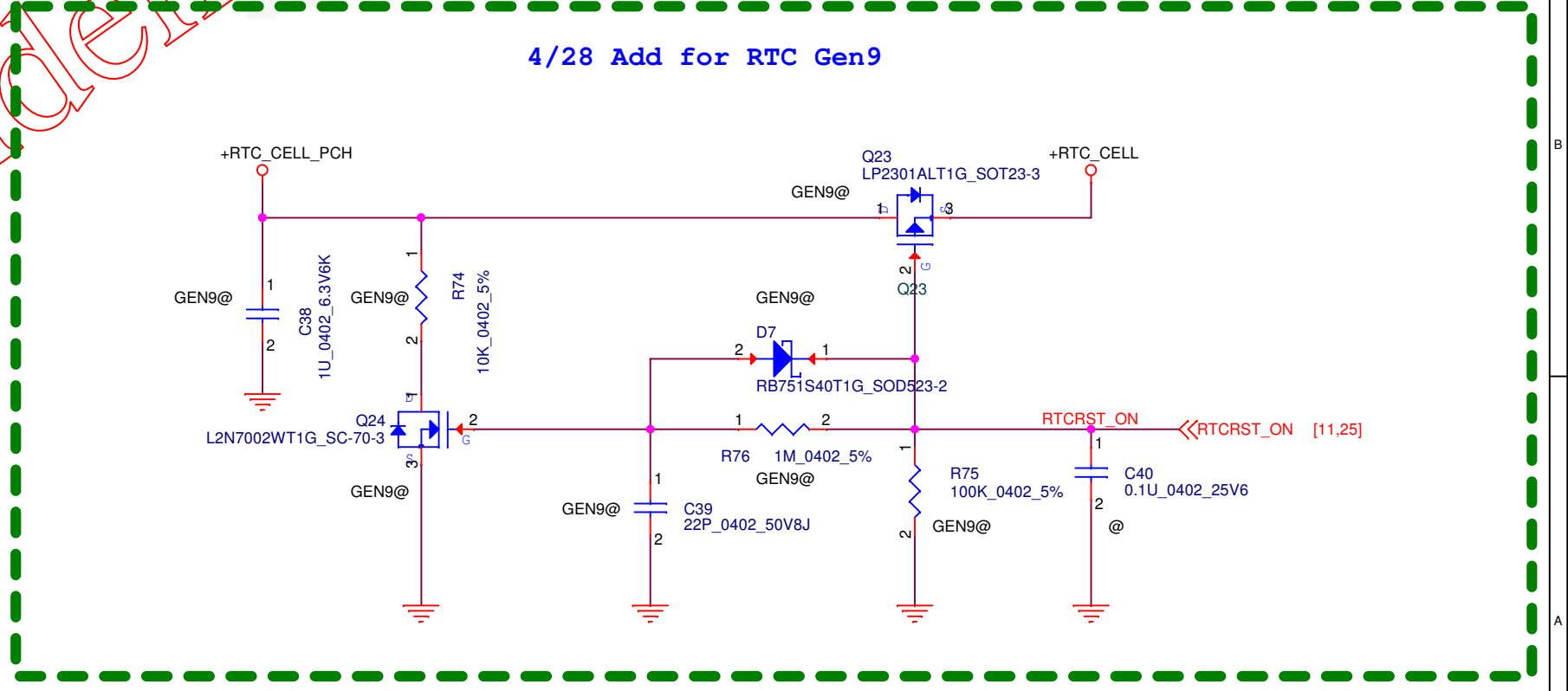
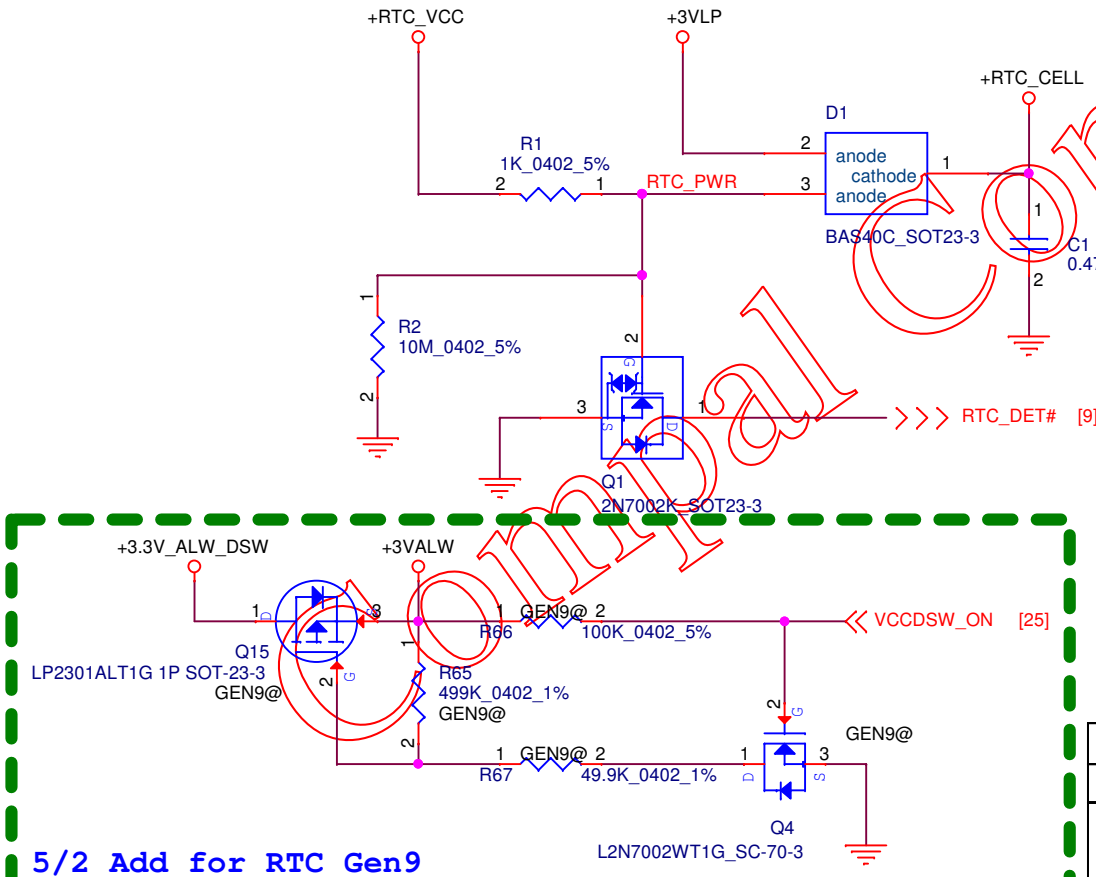


H12 WLAN STANDOFF

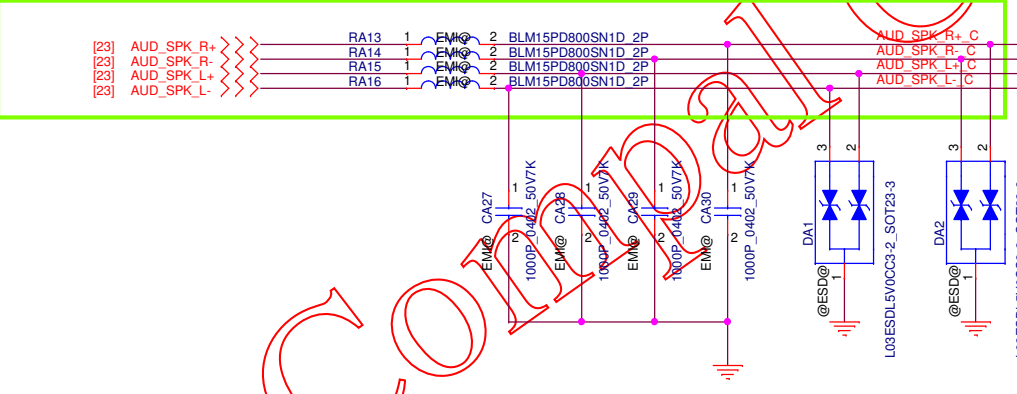
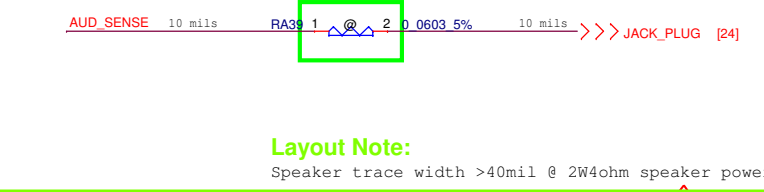
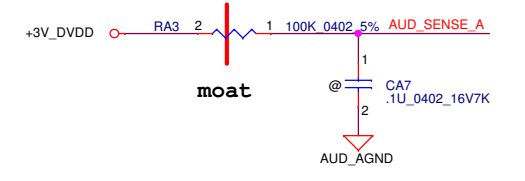
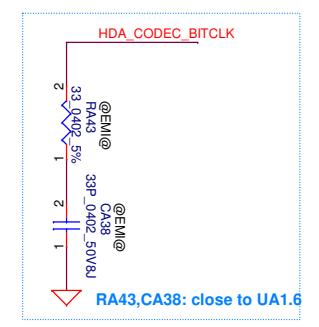
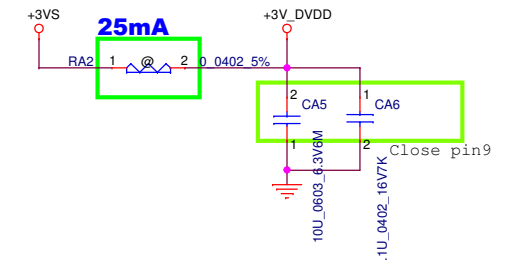
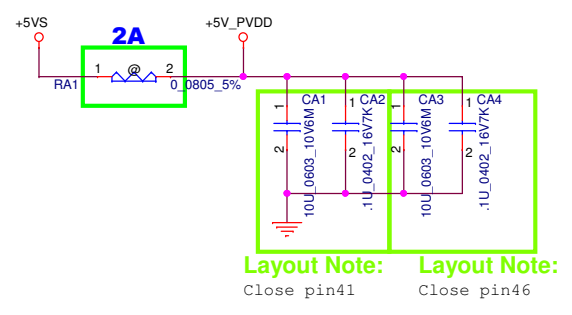


	Mounted	Unmounted	Comments
NPCT65x	RX5, RX7	RX6	VDD_VHIO - V_RUN Power VHIO - V_SPI Power
NPCT75x	RX6	RX5, RX7	VDD_VHIO and VHIO - V_RUN Power

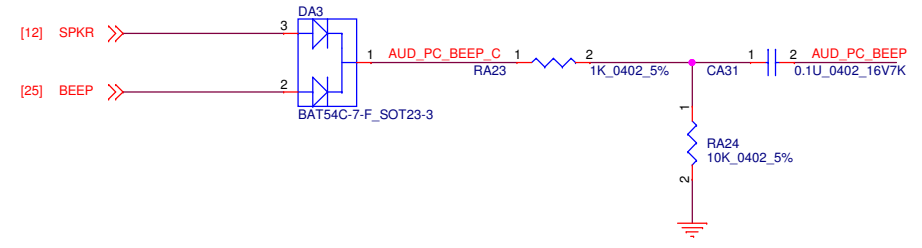
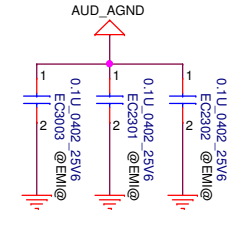
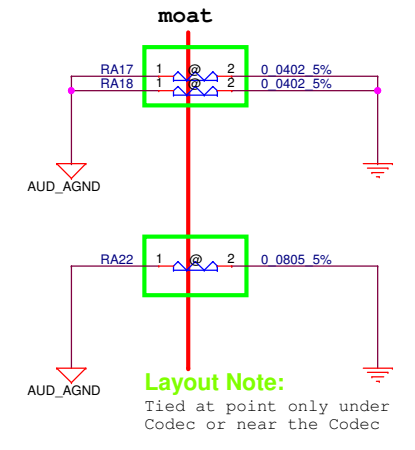
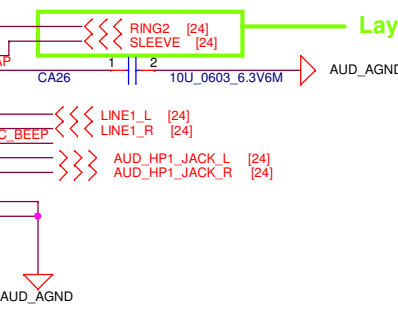
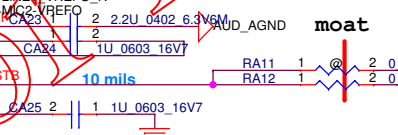
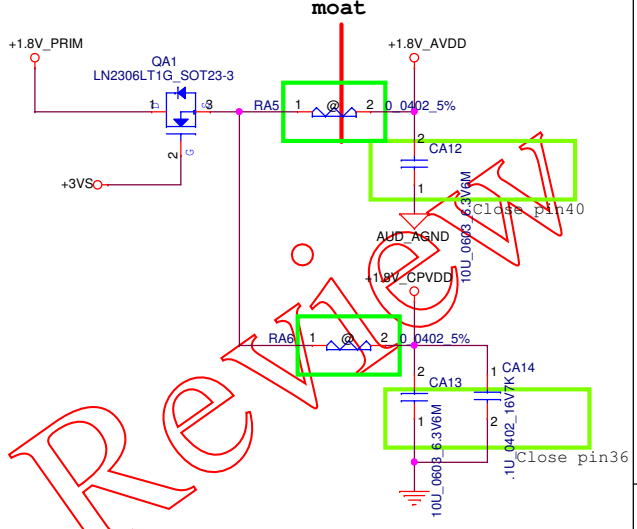
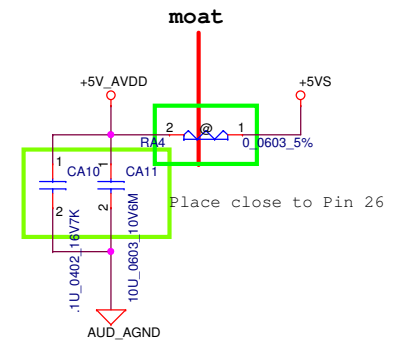
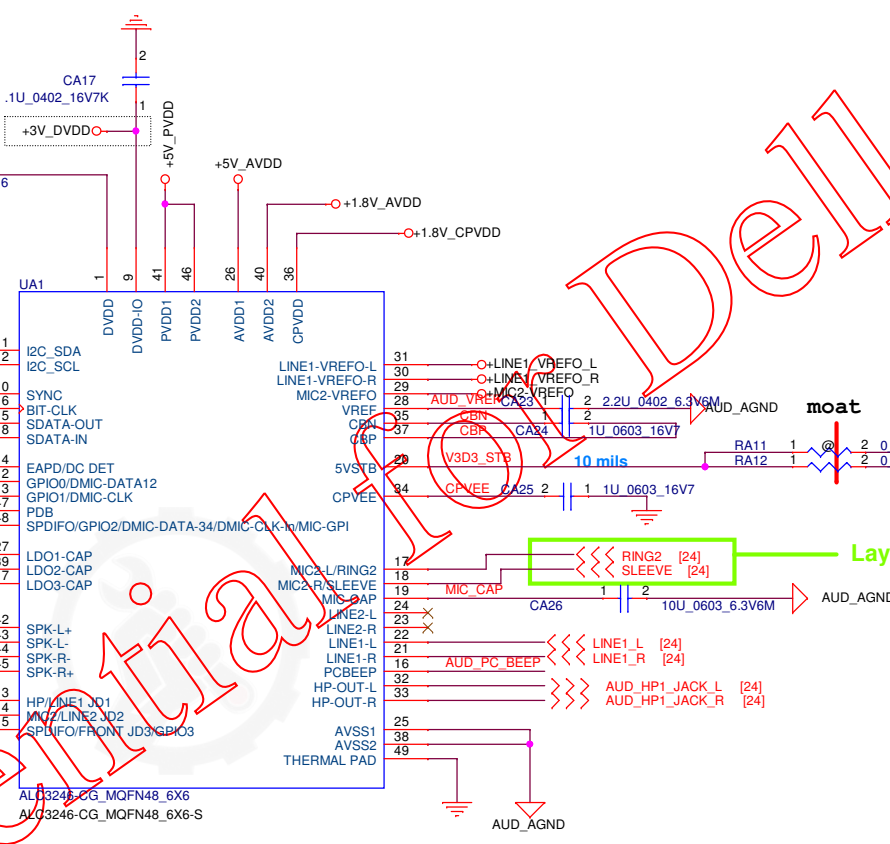
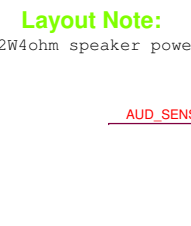
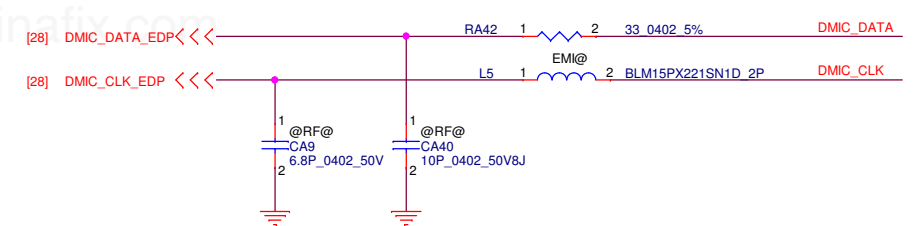
Main Func = RTC



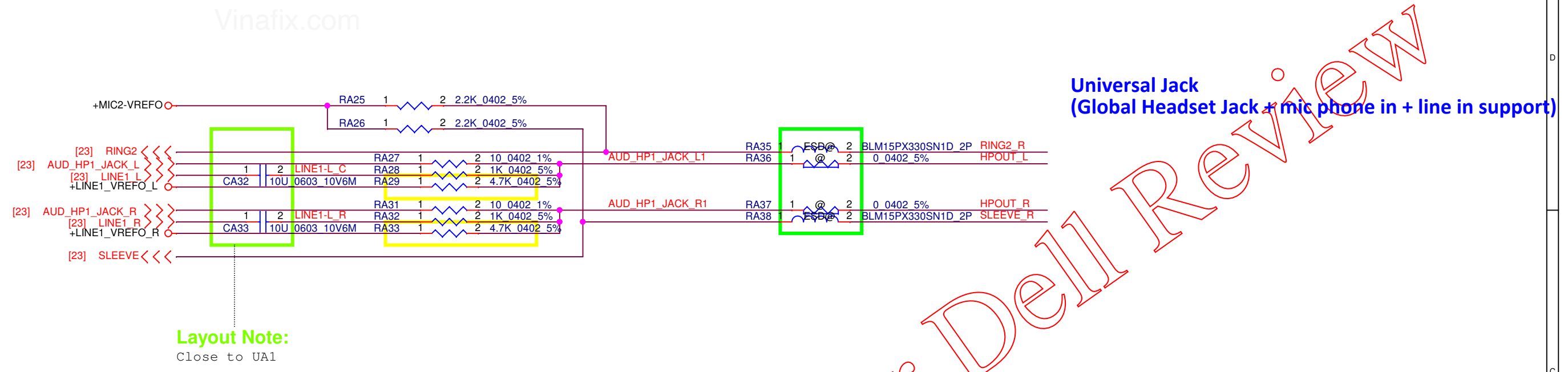
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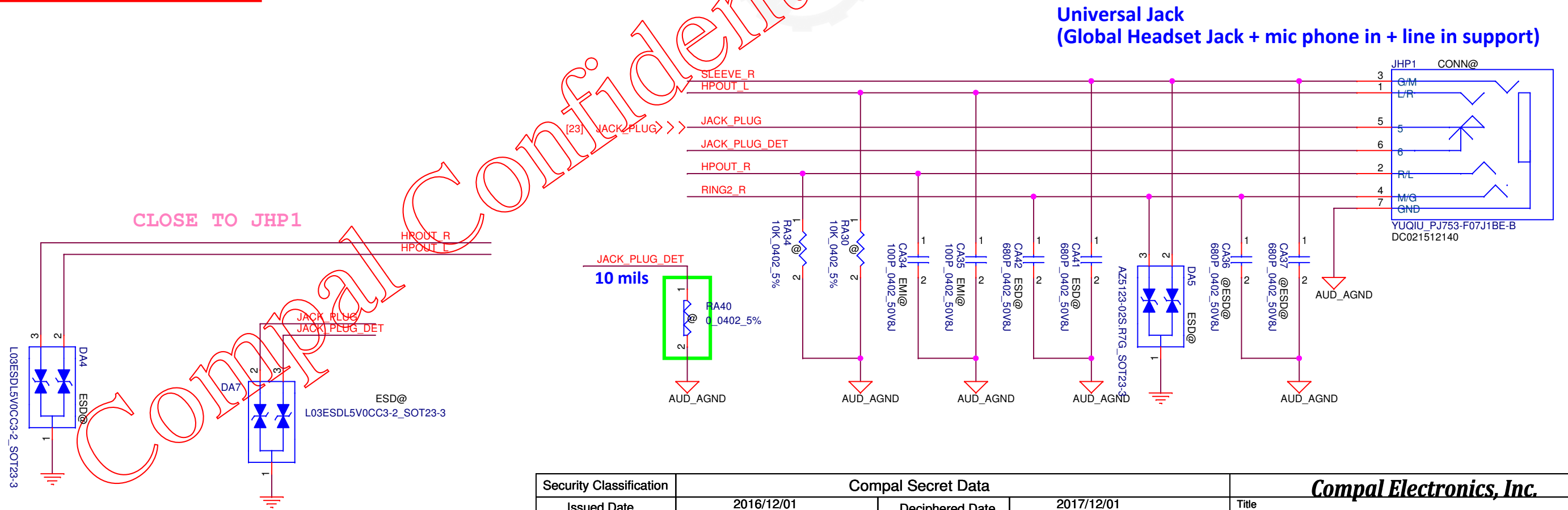
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Main Func = Audio Jack



Main Func = Audio Jack



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Main Func = EC

UE1 EC@
EC Chip CPN
 MEC1416-NU-D0_VTQFP128_14X14
SA0000A8L00

RE1 EC@
SD034499280
 For Board ID Select

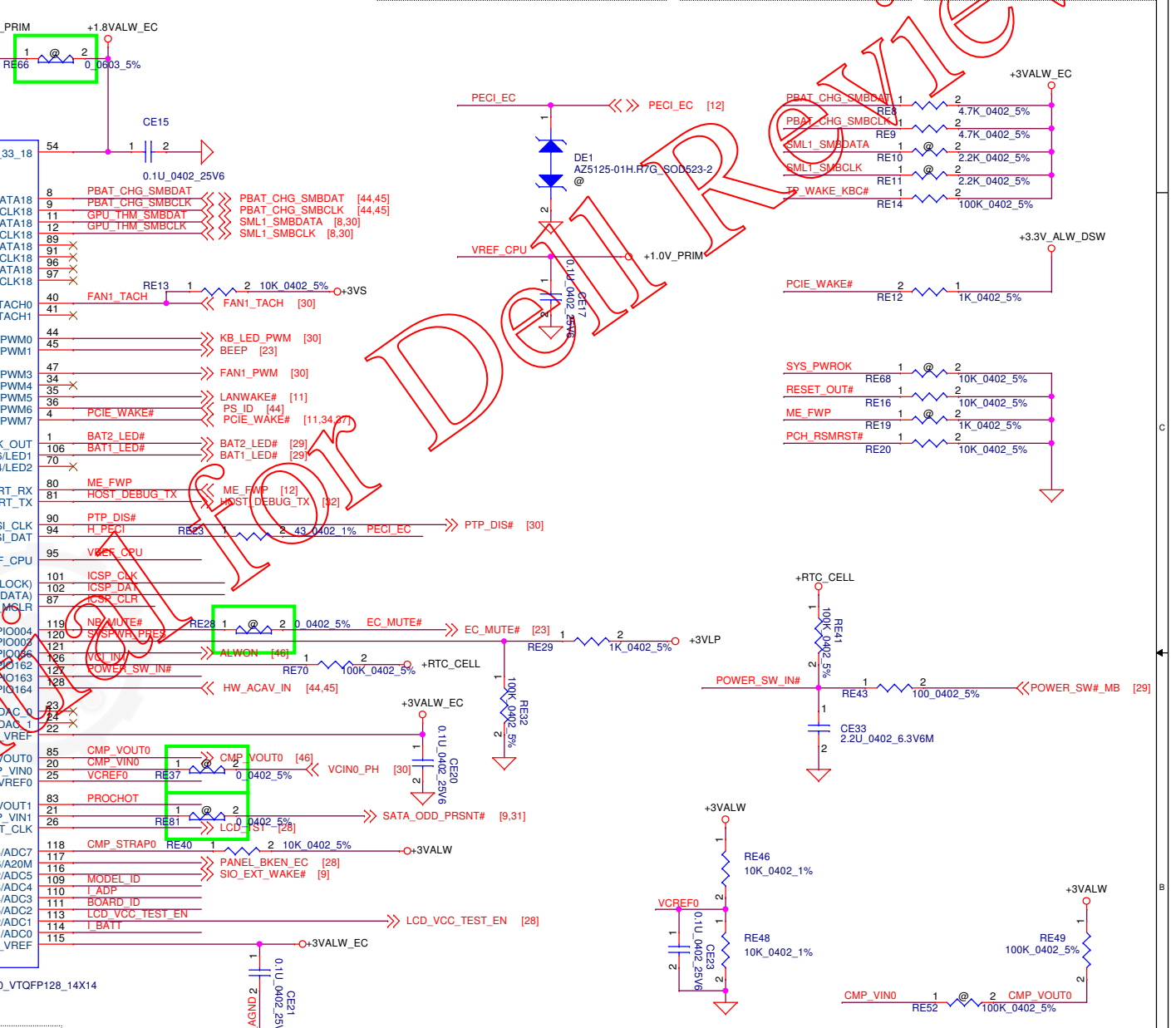
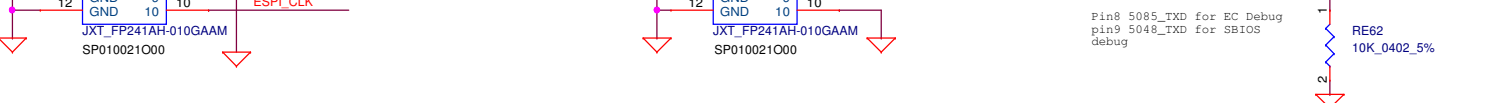
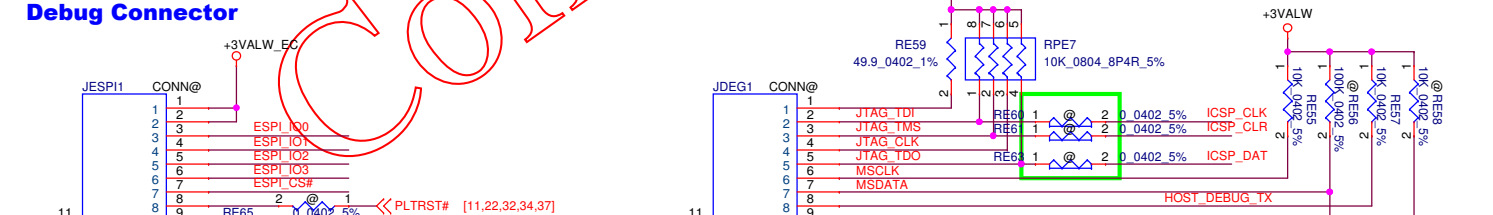
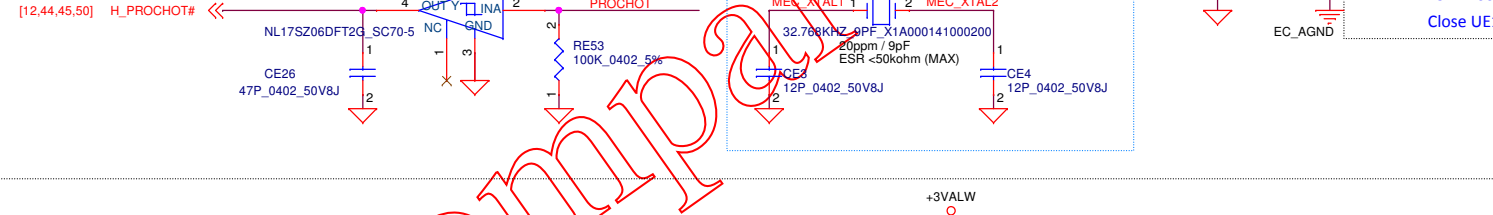
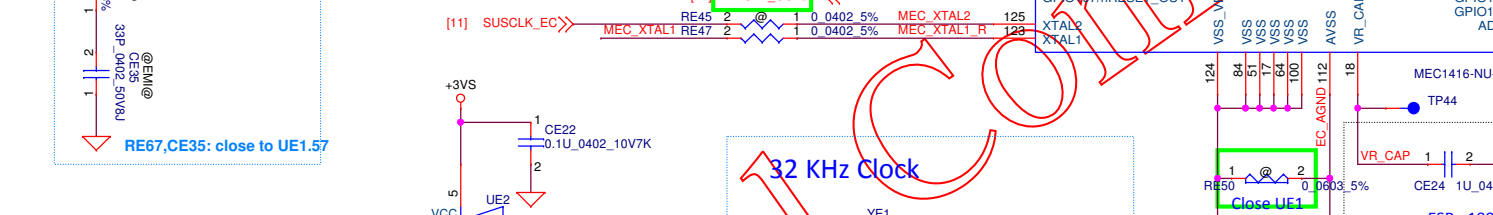
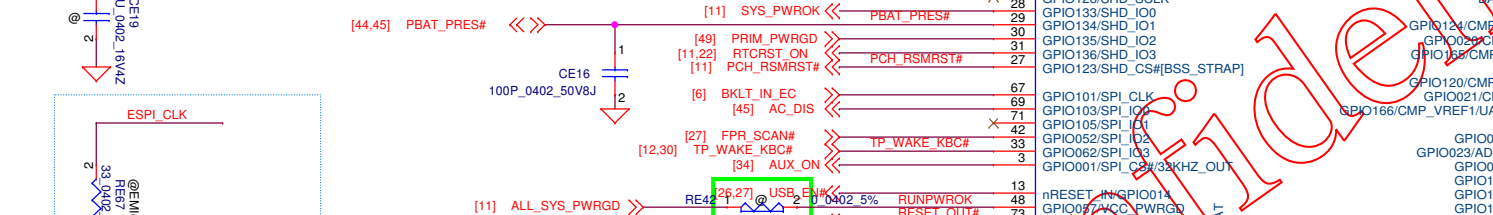
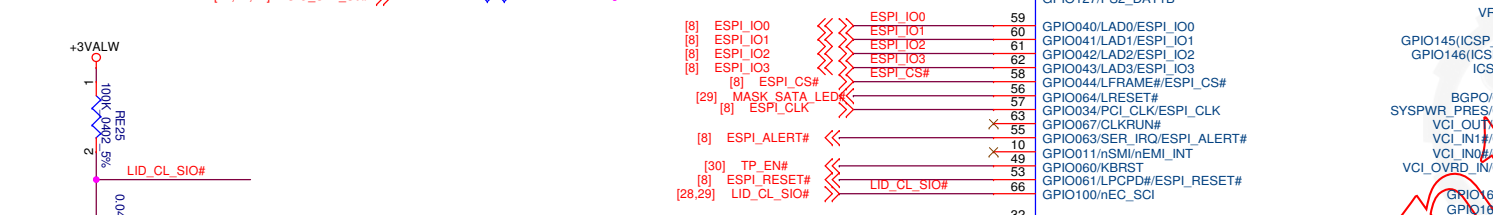
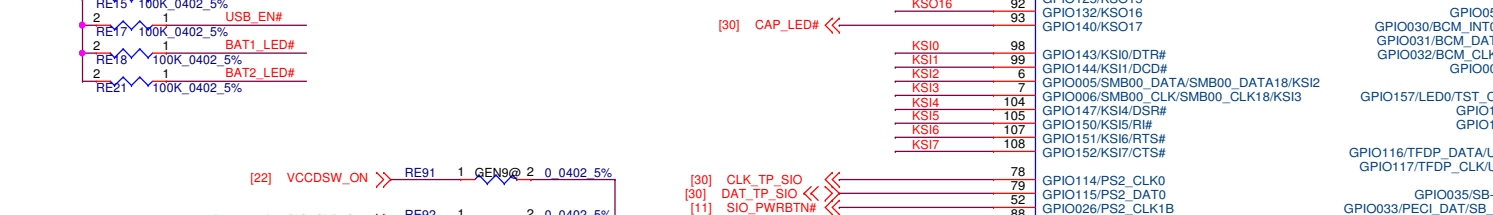
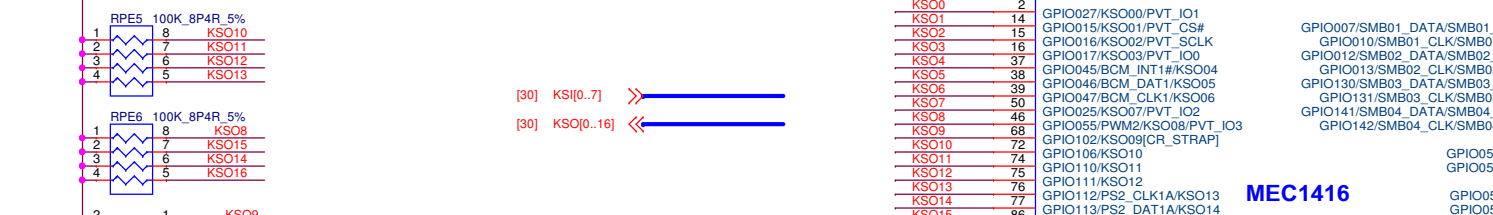
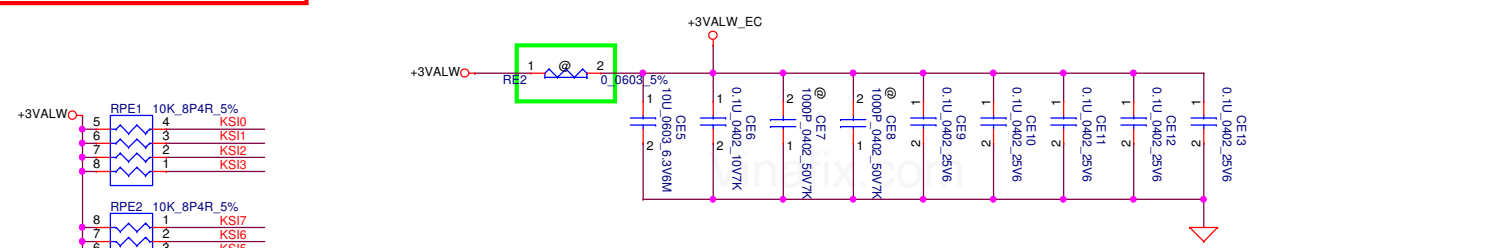
EVT	10K	SD034100380	100K_0402_1%
DVT1	17.8K	SD034154380	154K_0402_1%
DVT2	27K	SD034200380	200K_0402_1%
Pilot	49.9K	SD034232380	232K_0402_1%
		SD034100380	100K_0402_1%

Model ID

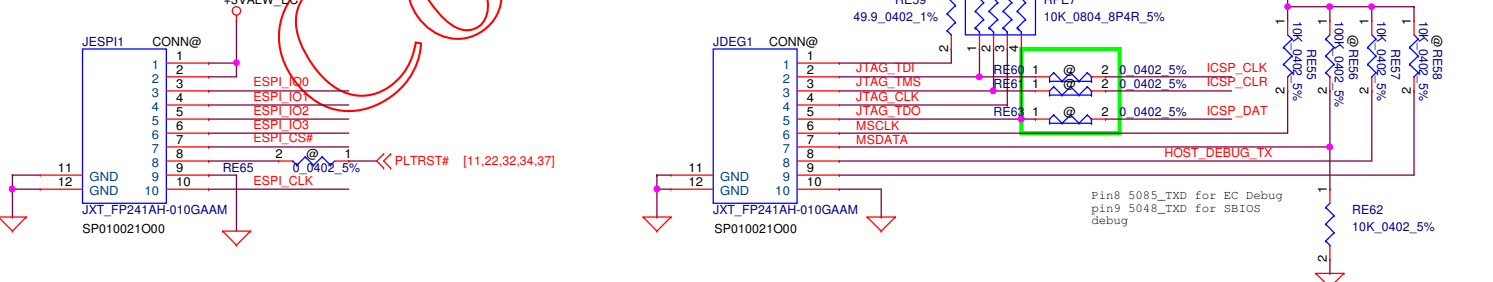
RE3 100K_0402_1%
 RE4 100K_0402_1%
 CE1 0.1U_0402_10V7K

Board ID

RE1 100K_0402_1%
 RE6 100K_0402_1%
 CE2 0.1U_0402_10V7K

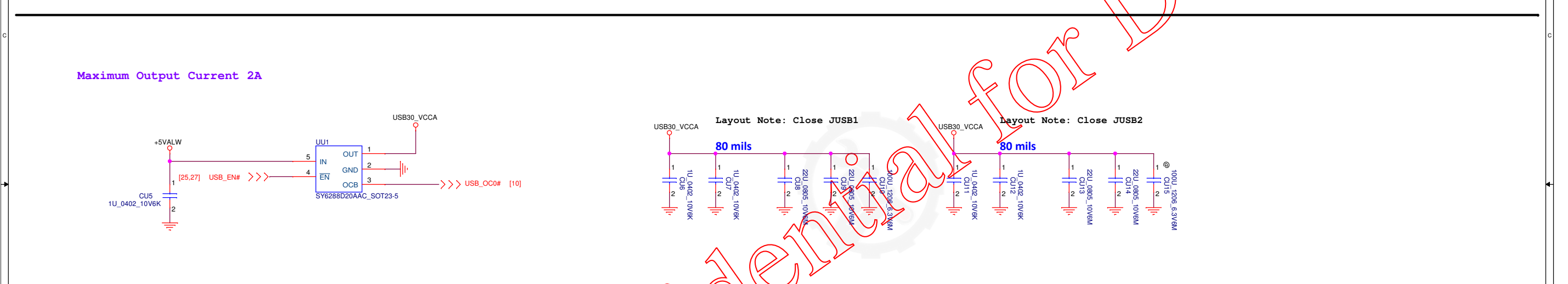
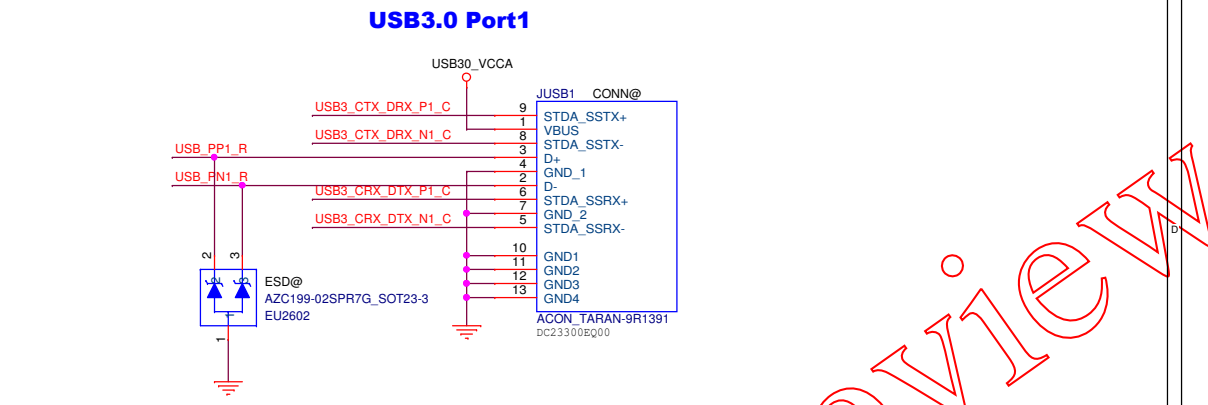
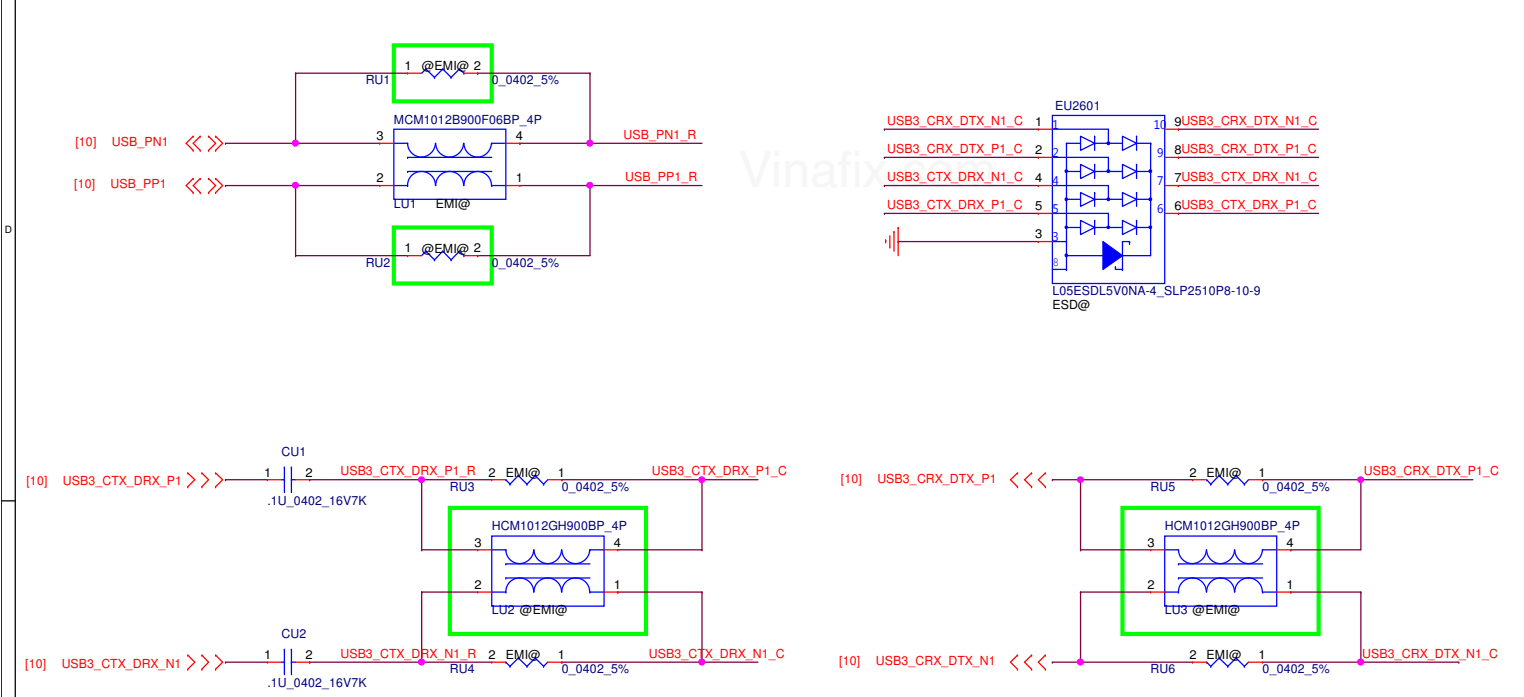


Debug Connector

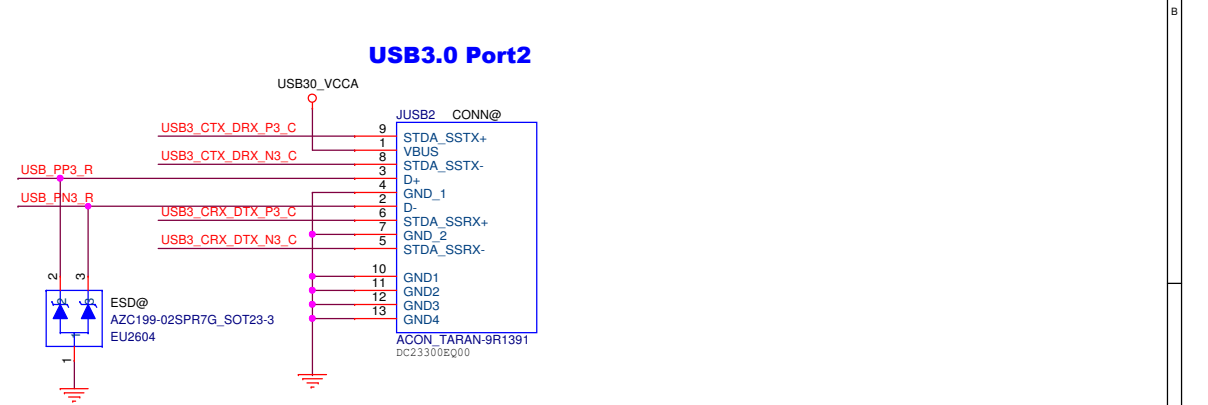
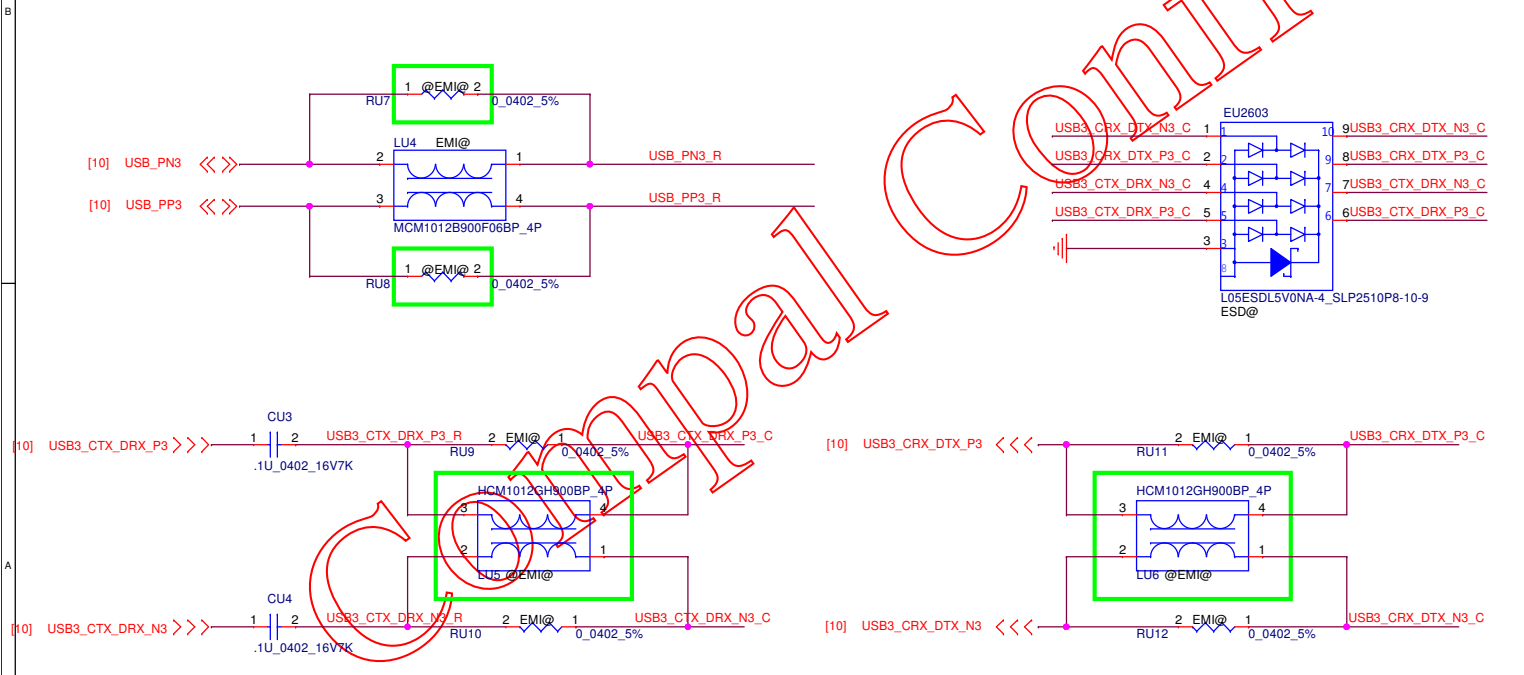


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		2017/12/01
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	EC MEC1416	
Size	Document Number	Rev
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Main Func = USB3.0 Port1



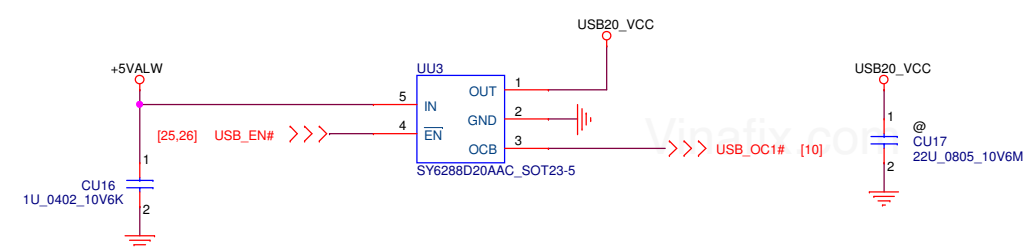
Main Func = USB3.0 Port2



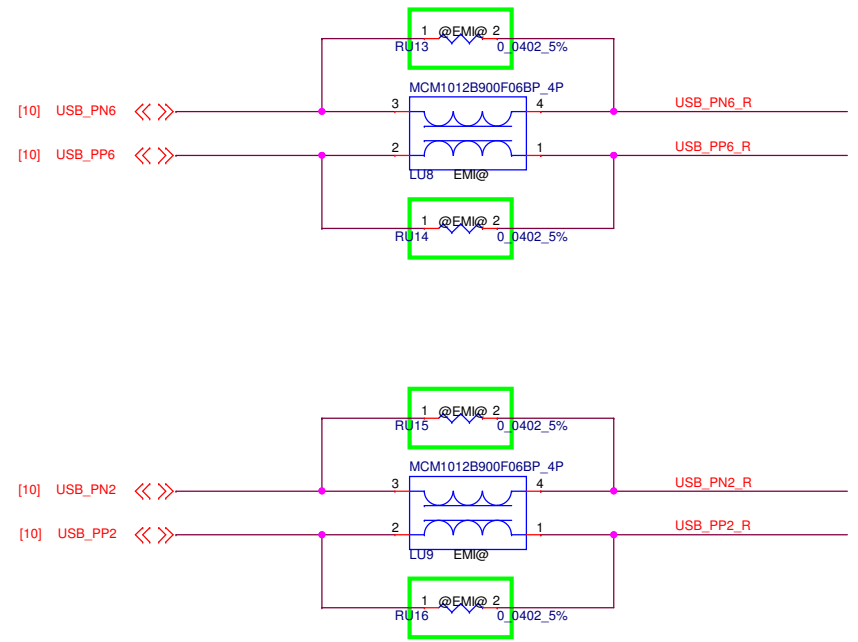
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Issued Date	2016/12/01	Deciphered Date	2017/12/01	Title
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Main Func = USB2.0 + Card Reader on IO/B

SY6288D Support 2A

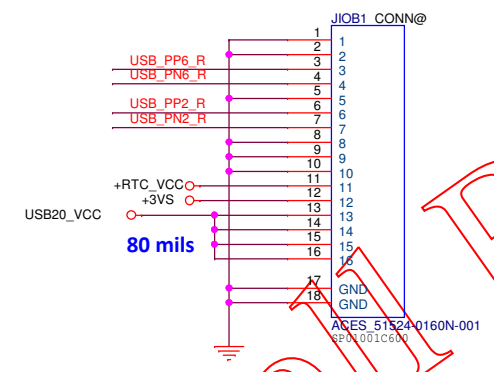


CardReader

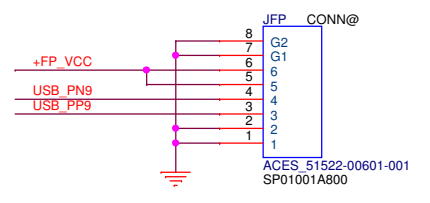
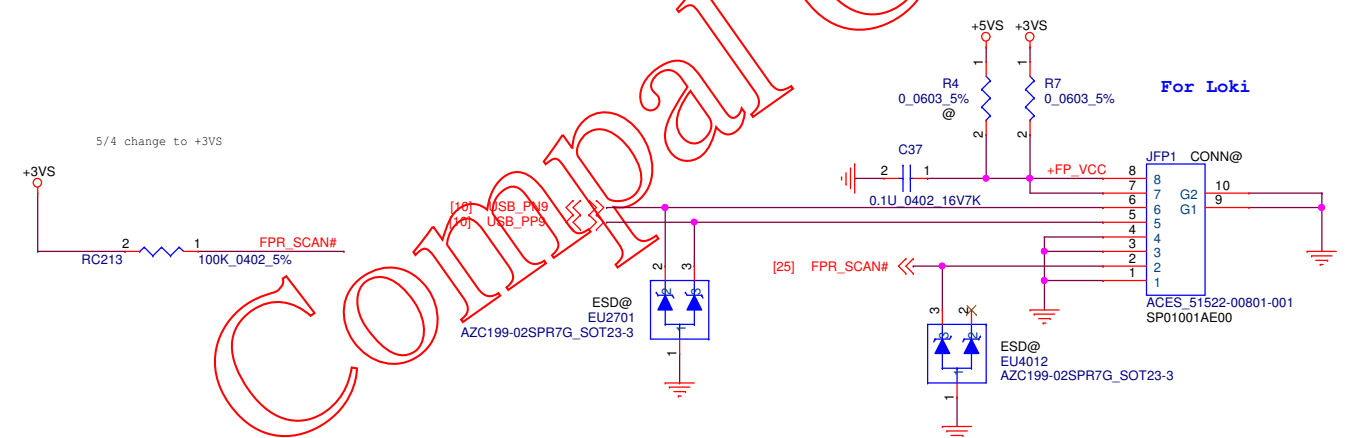


I/O Board Connector

CardReader



Main Func = Finger Printer

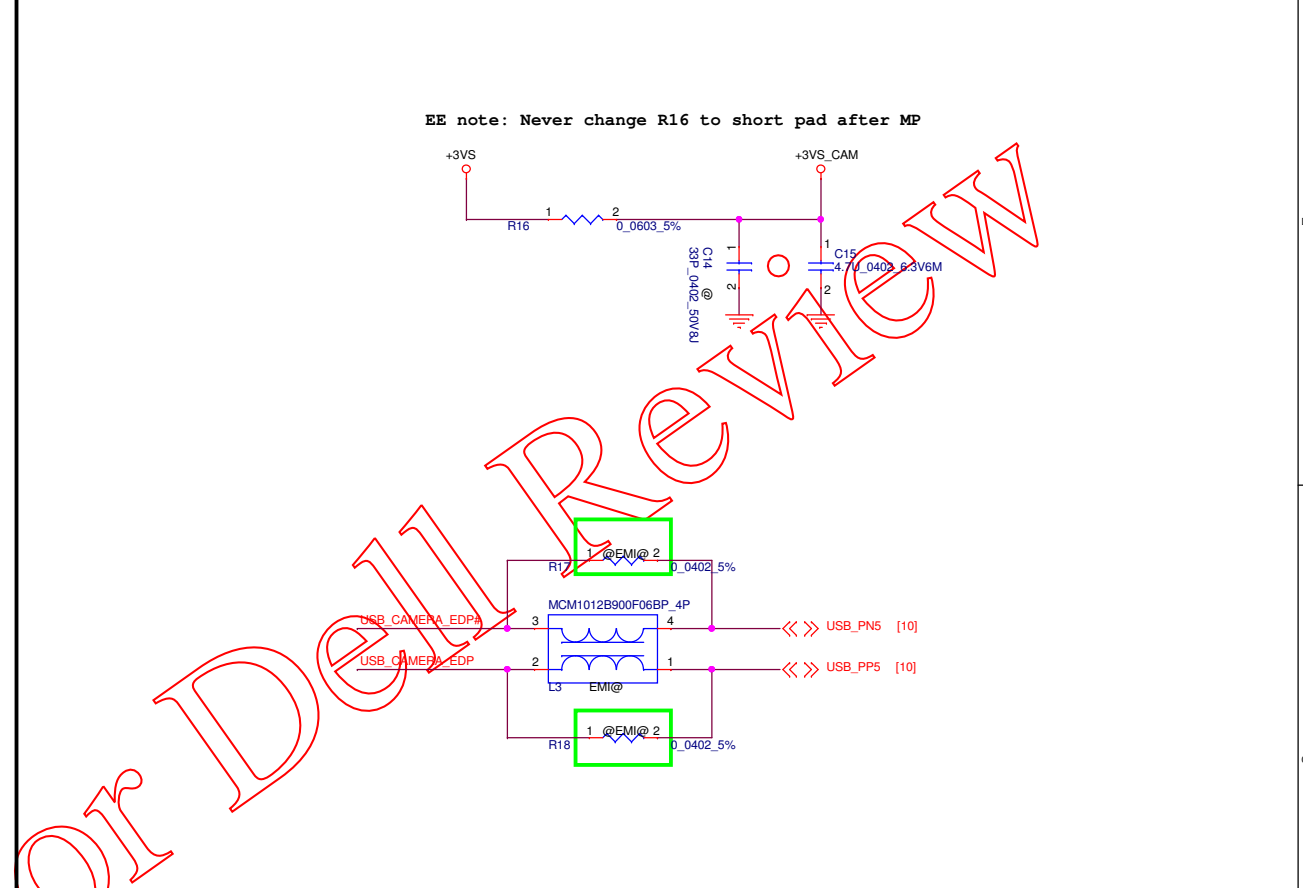
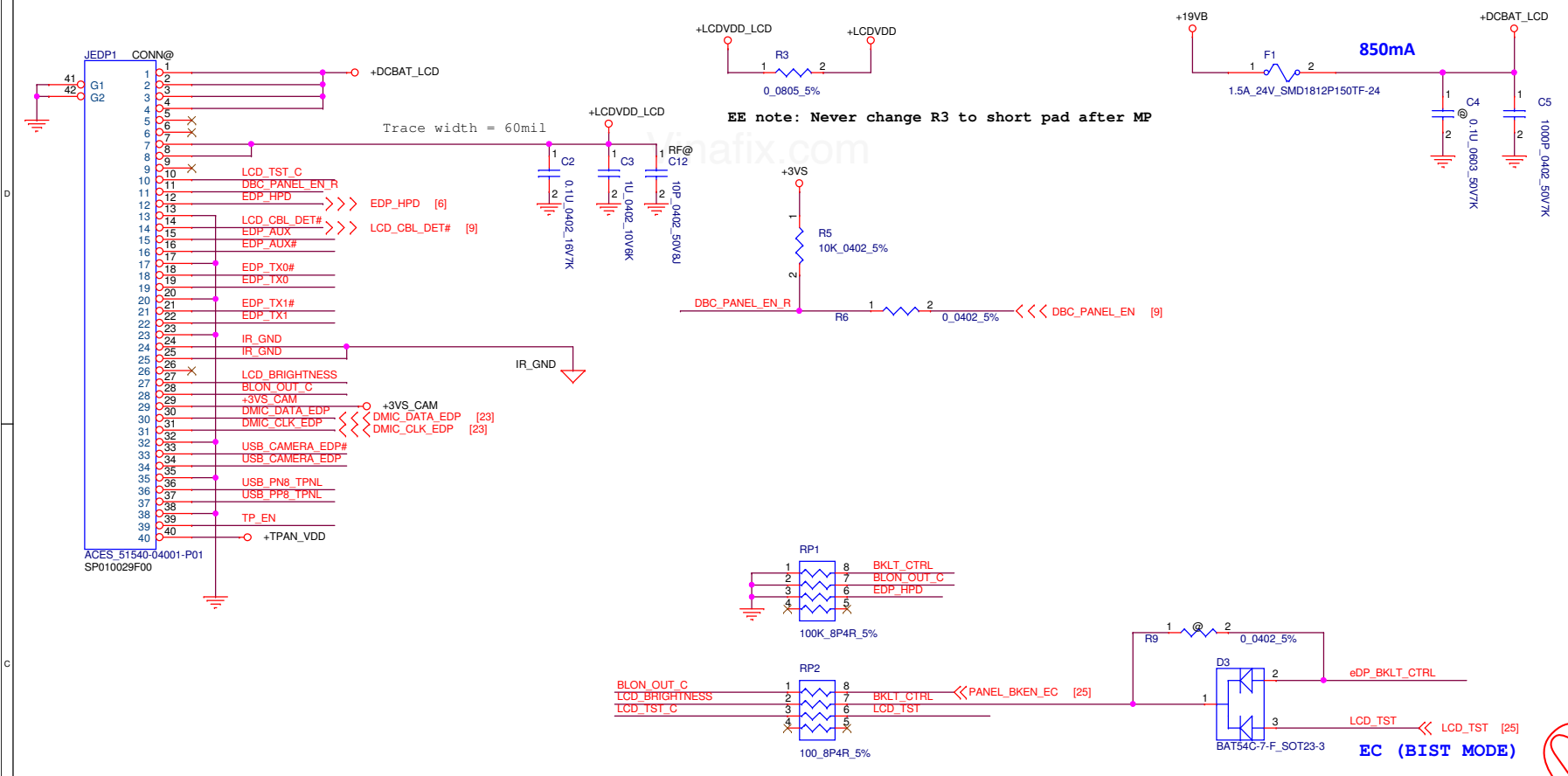


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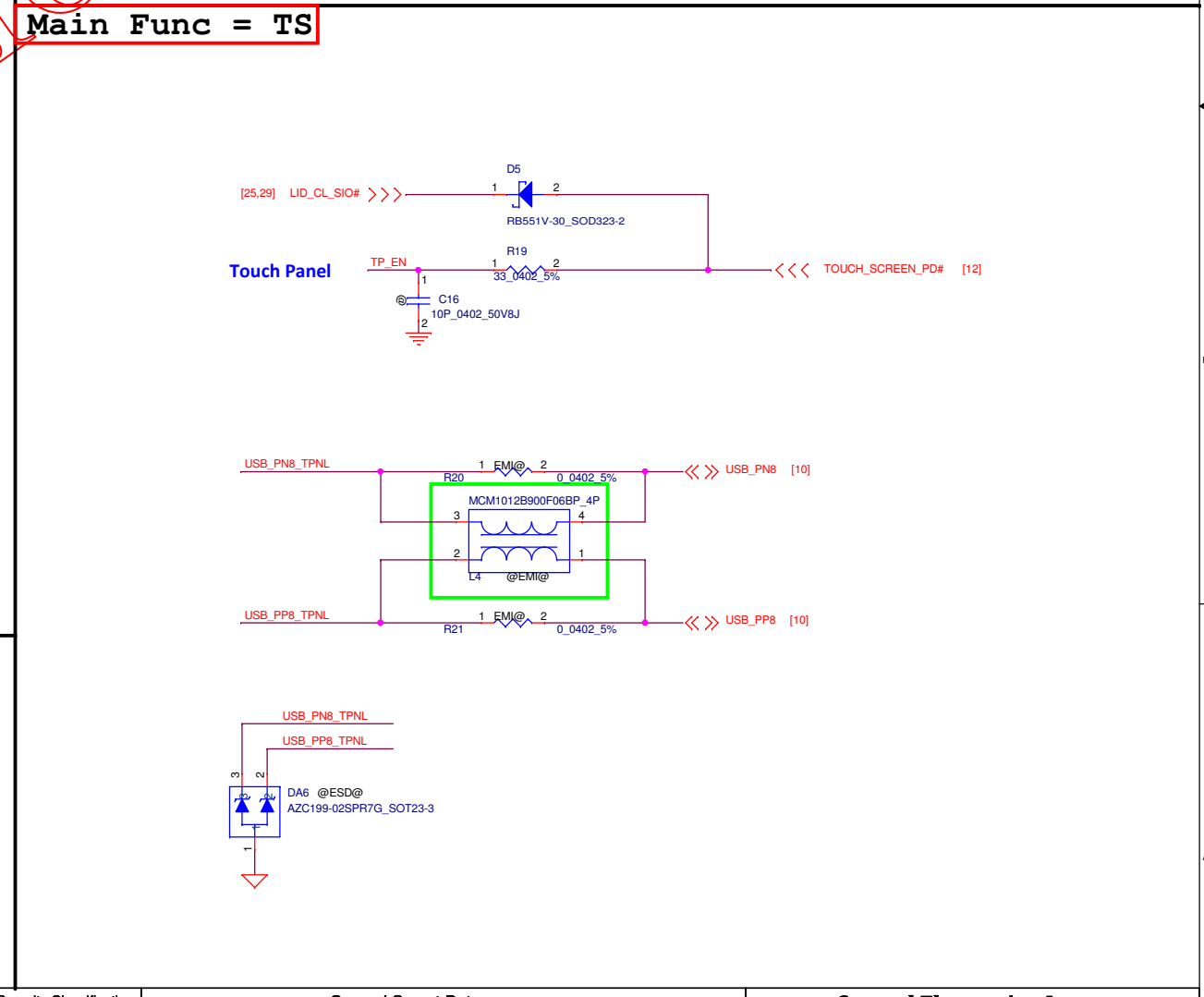
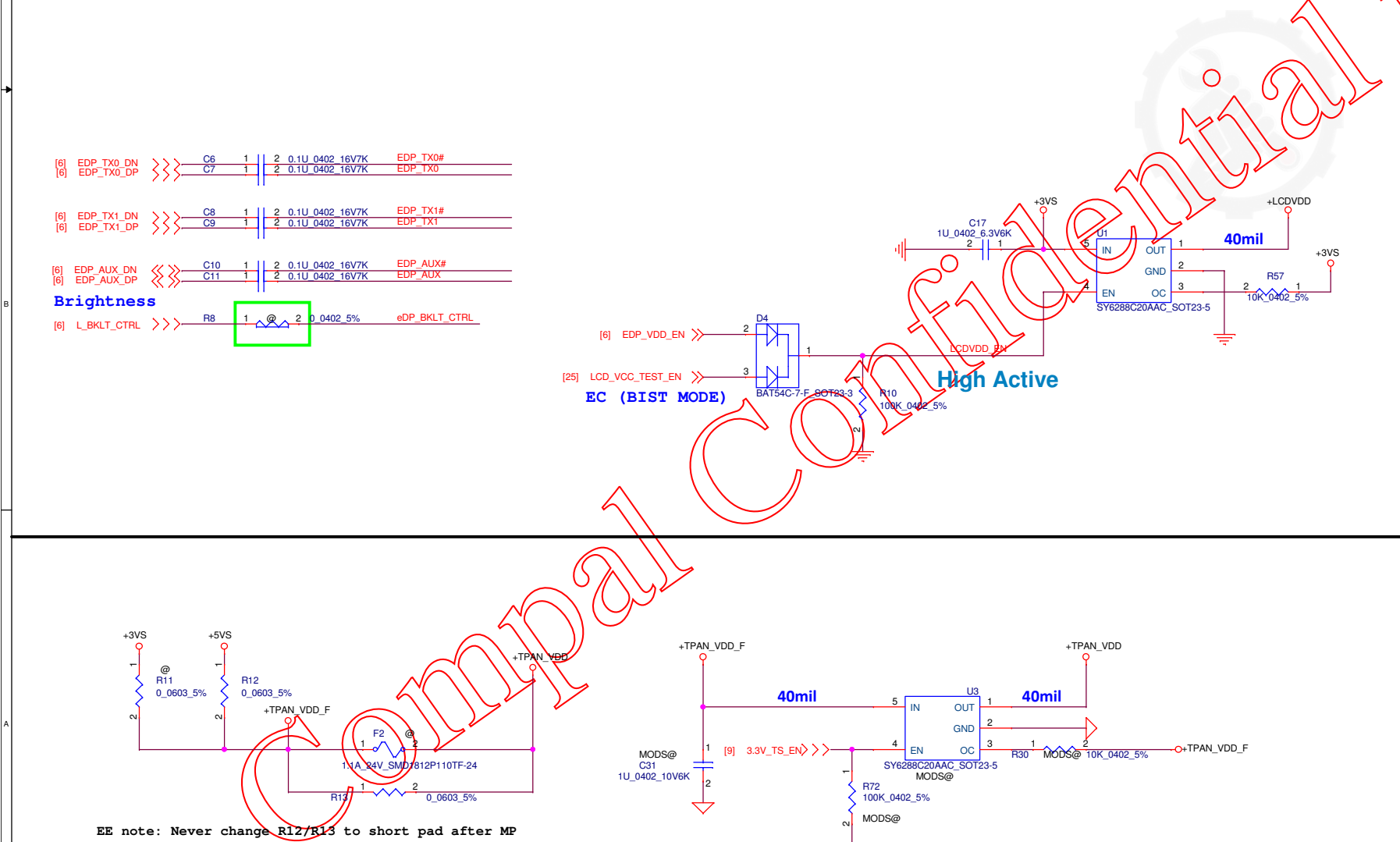
Main Func = LCD

INVERTER POWER

Main Func = CAM

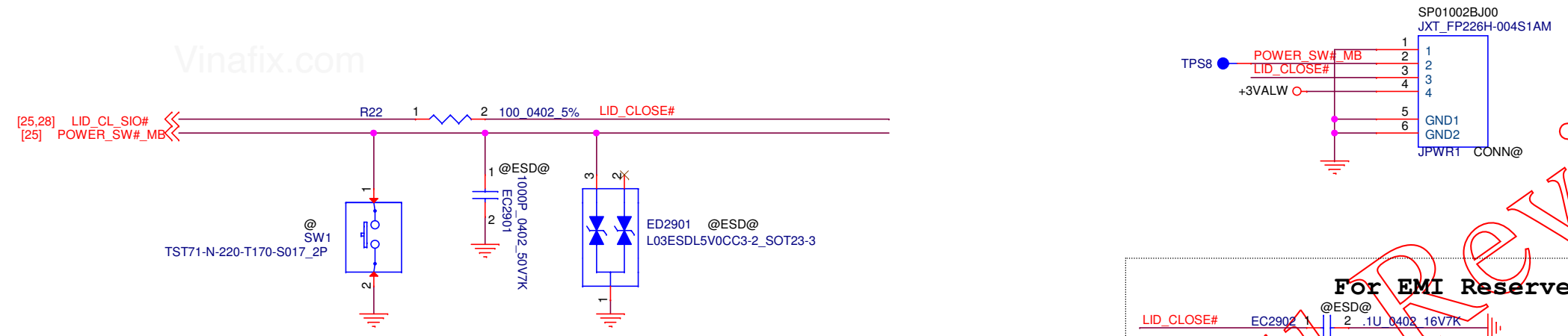


Main Func = TS



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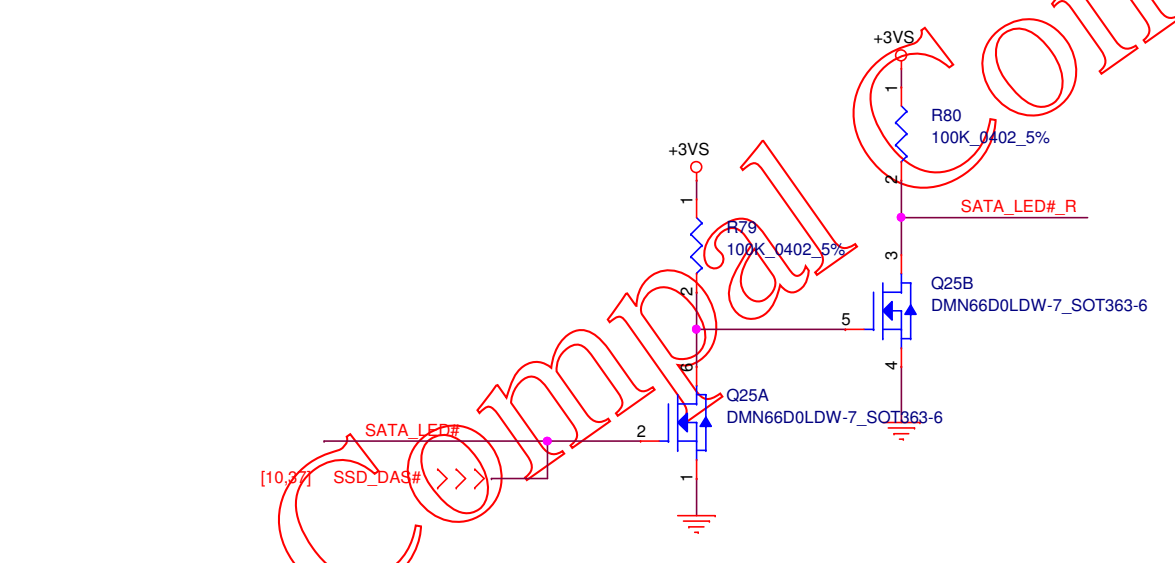
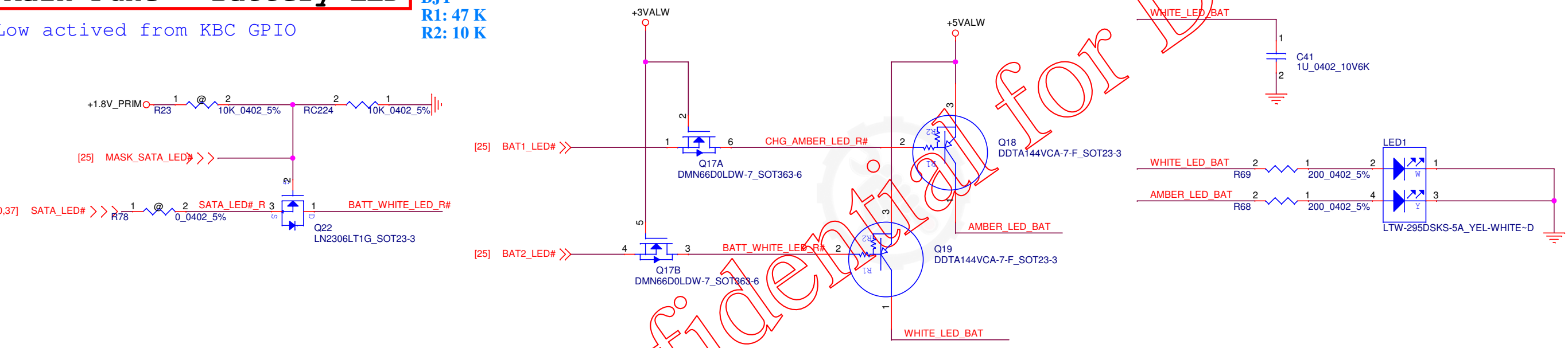
Main Func = Power BTN



Main Func = Battery LED

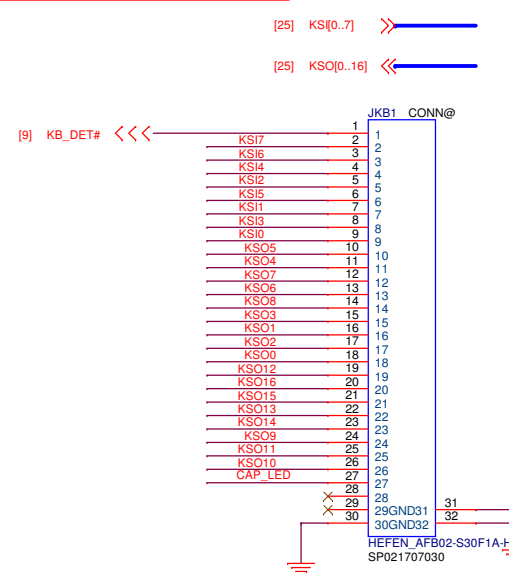
Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K

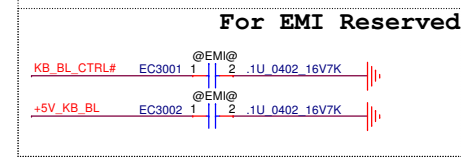
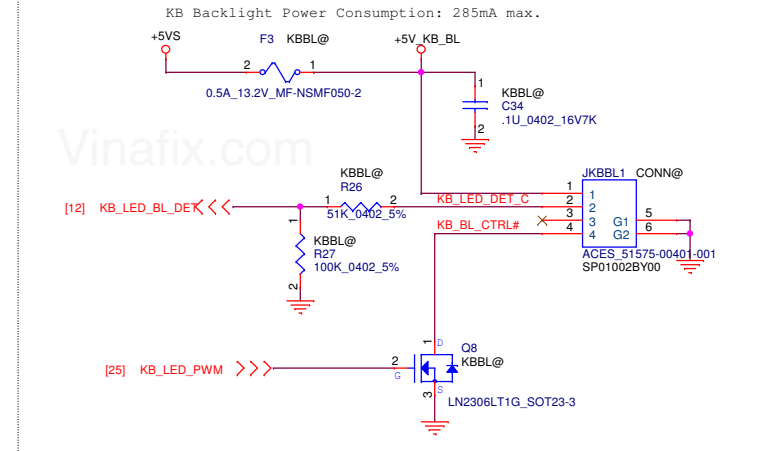


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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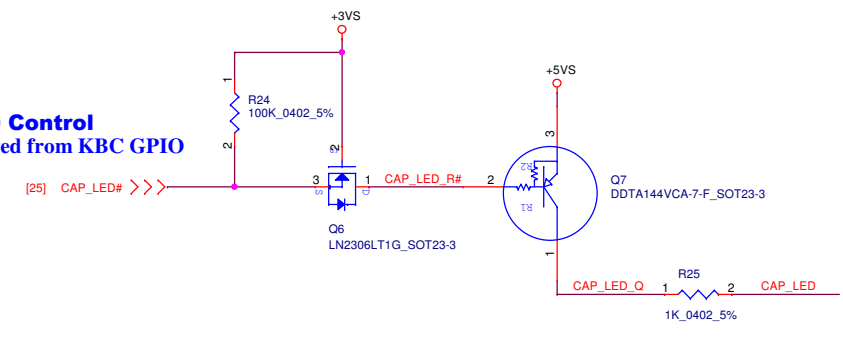
Main Func = KB



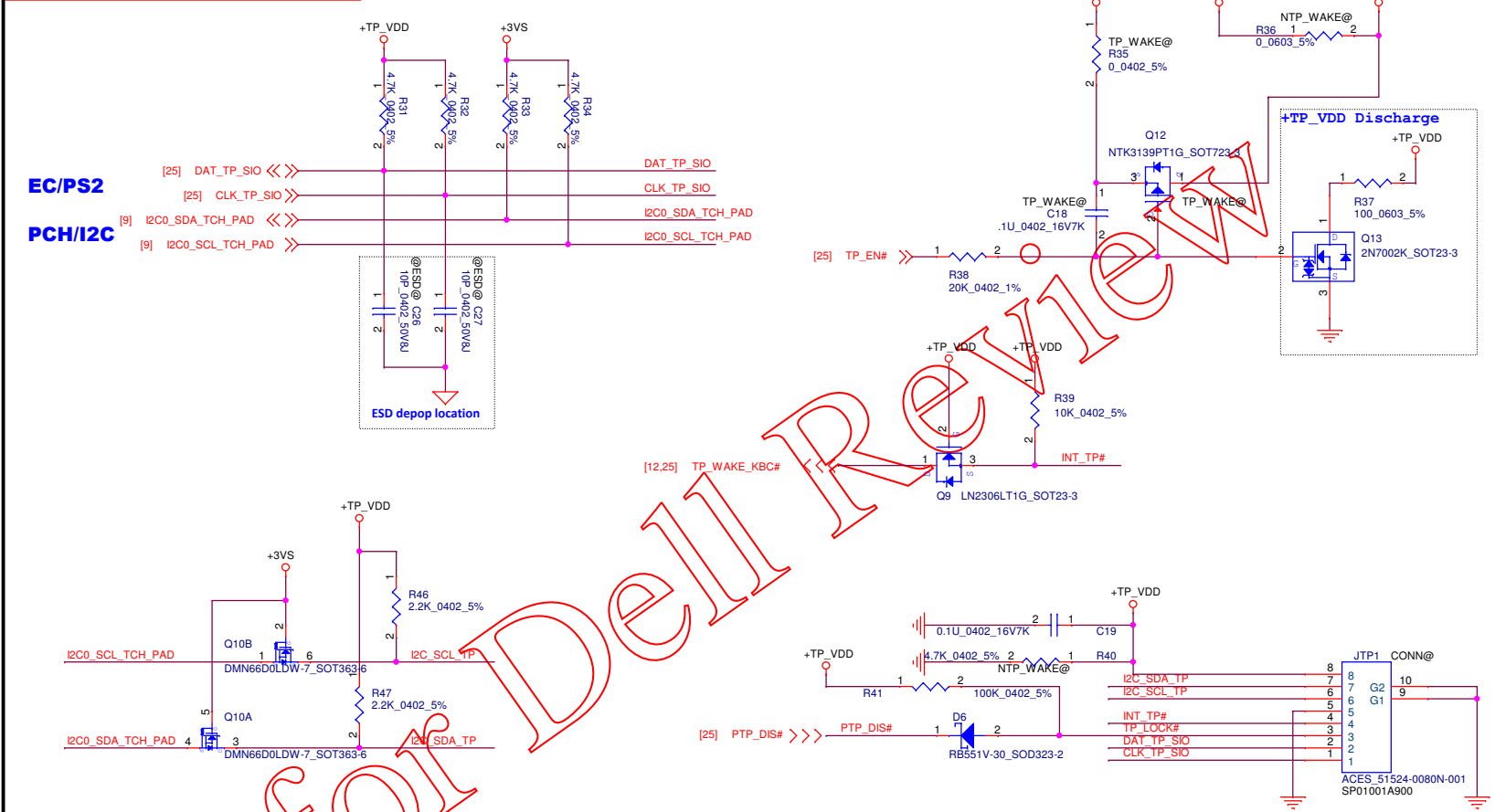
Keyboard Backlight (Reserved)



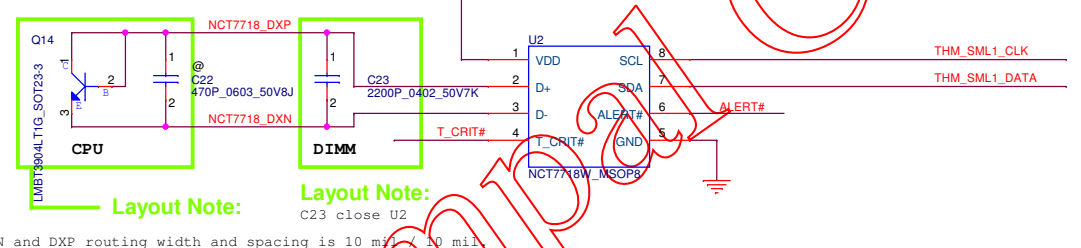
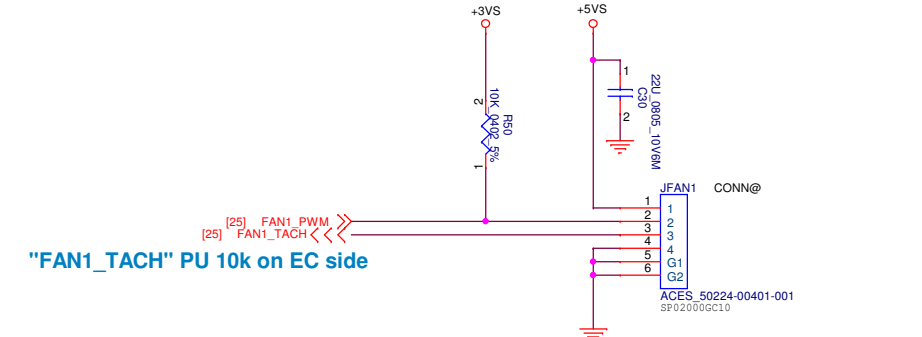
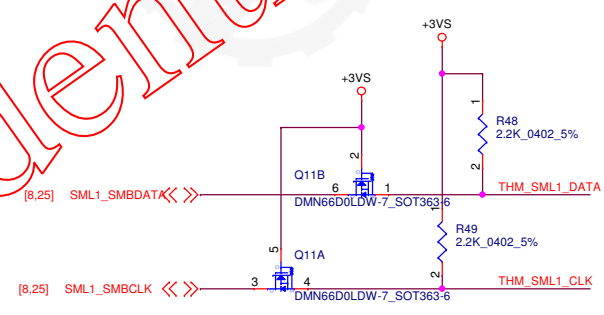
CAP LED Control
LOW acted from KBC GPIO



Main Func = TPAD

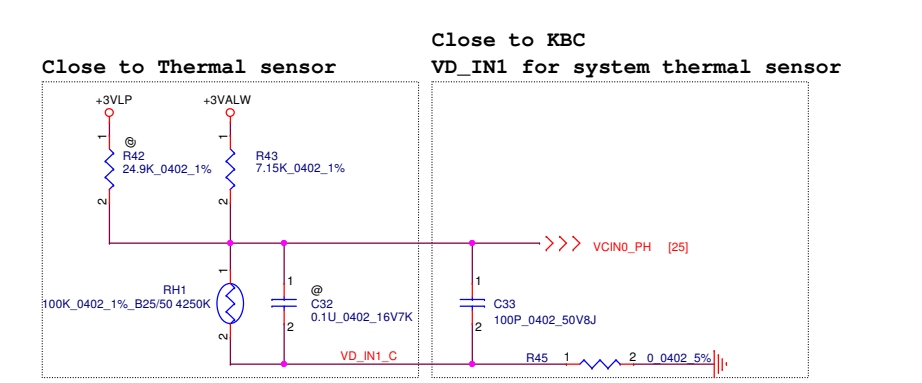


Main Func = Thermal

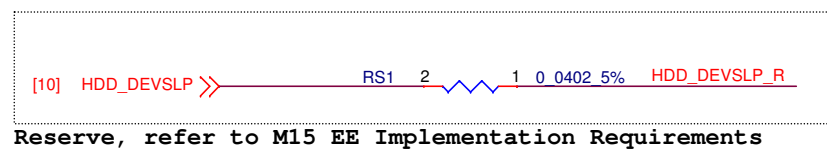
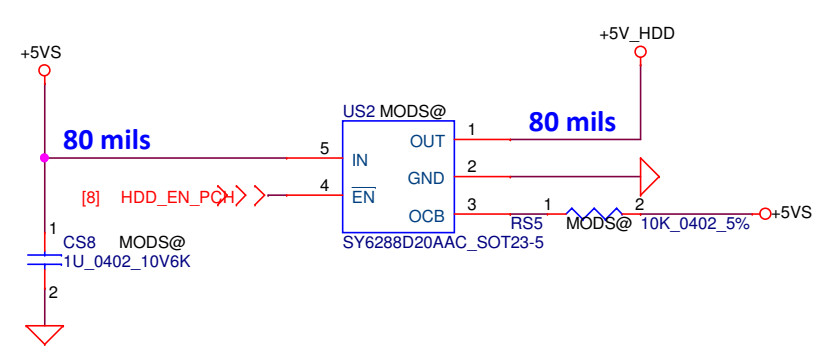
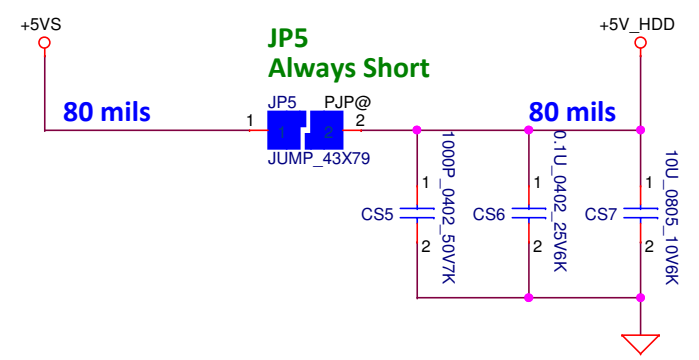


TEMPERATURE (°C)	T_CRIT#					
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ	
ALERT#	77	87	97	107	117	
	79	89	99	109	119	
	81	91	101	111	121	
	83	93	103	113	123	
	85	95	105	115	125	

Main Func = OTP



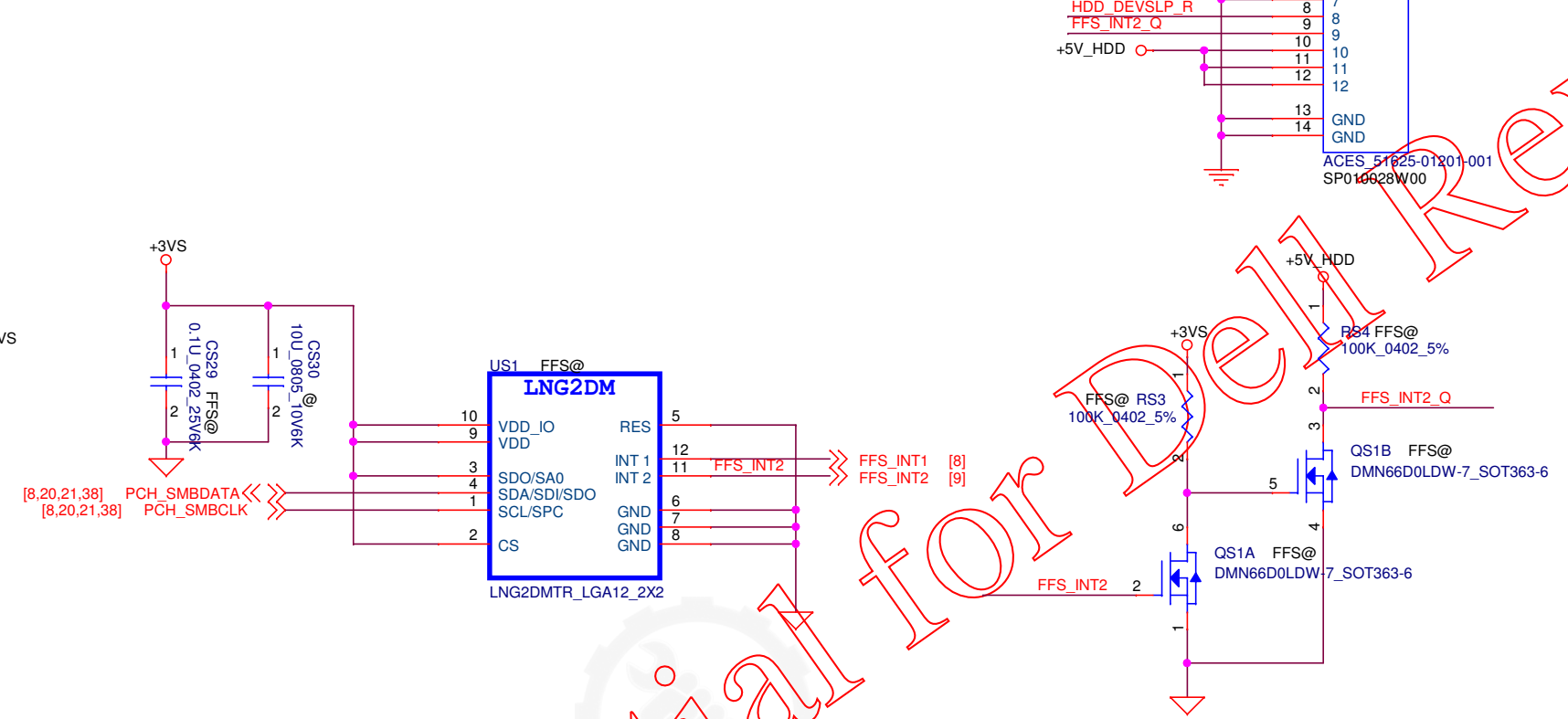
Main Func = HDD&FFS



Reserve, refer to M15 EE Implementation Requirements

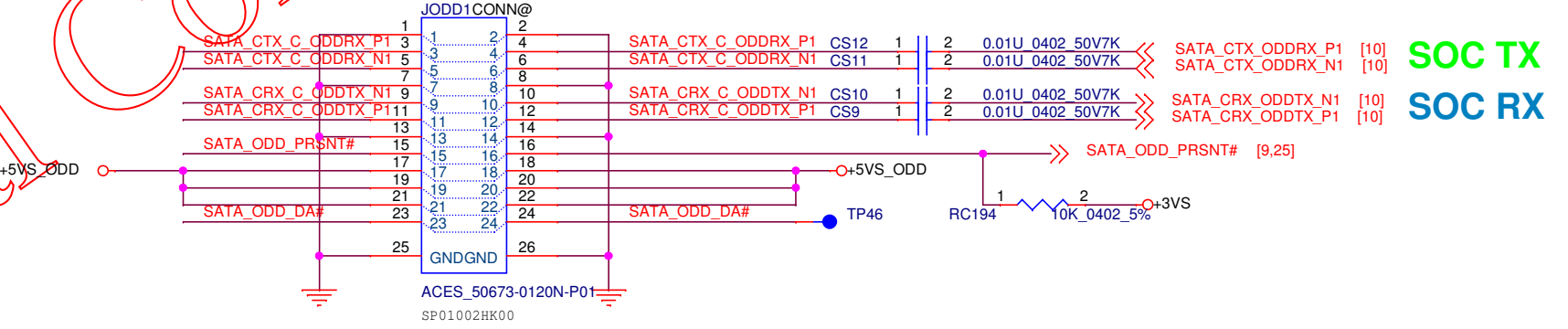
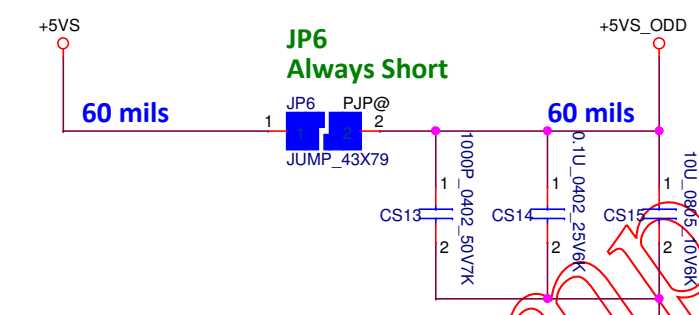
SOC TX [10] SATA3_CTX_HDDR_X_P0
[10] SATA3_CTX_HDDR_X_N0

SOC RX [10] SATA3_CRX_HDDTX_N0
[10] SATA3_CRX_HDDTX_P0



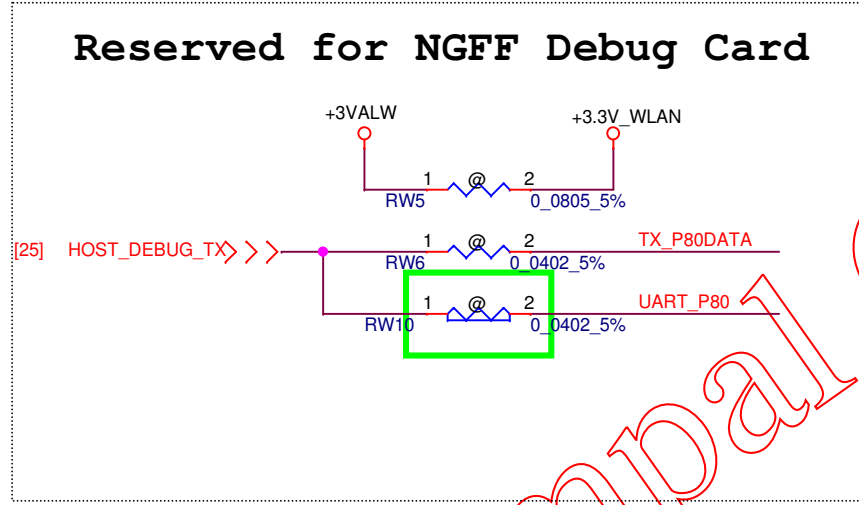
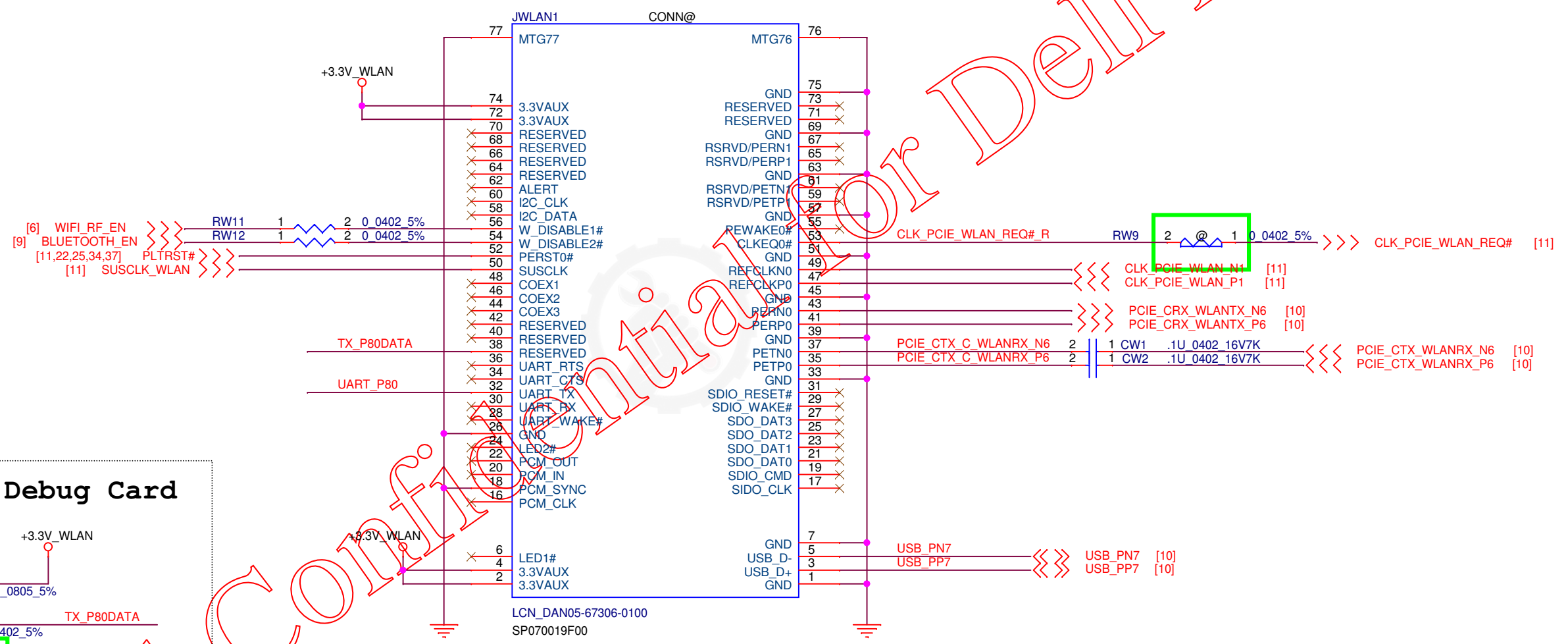
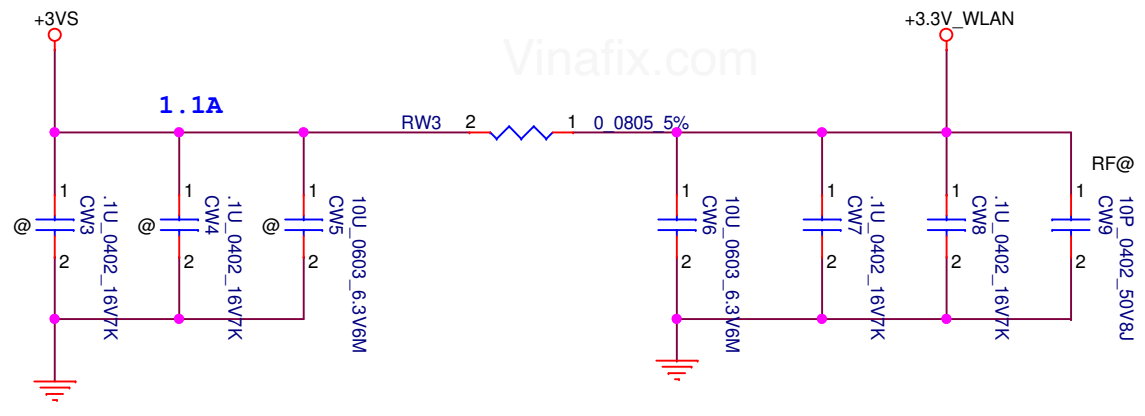
CONN	FFC
GND	S1 1
A+	S2 2
A-	S3 3
GND	S4 4
B-	S5 5
B+	S6 6
GND	S7 7
DEVSLP	P3
5V	P7 10
5V	P8 11
5V	P9 12
GND	P10
Device Activity	P11

Main Func = ODD



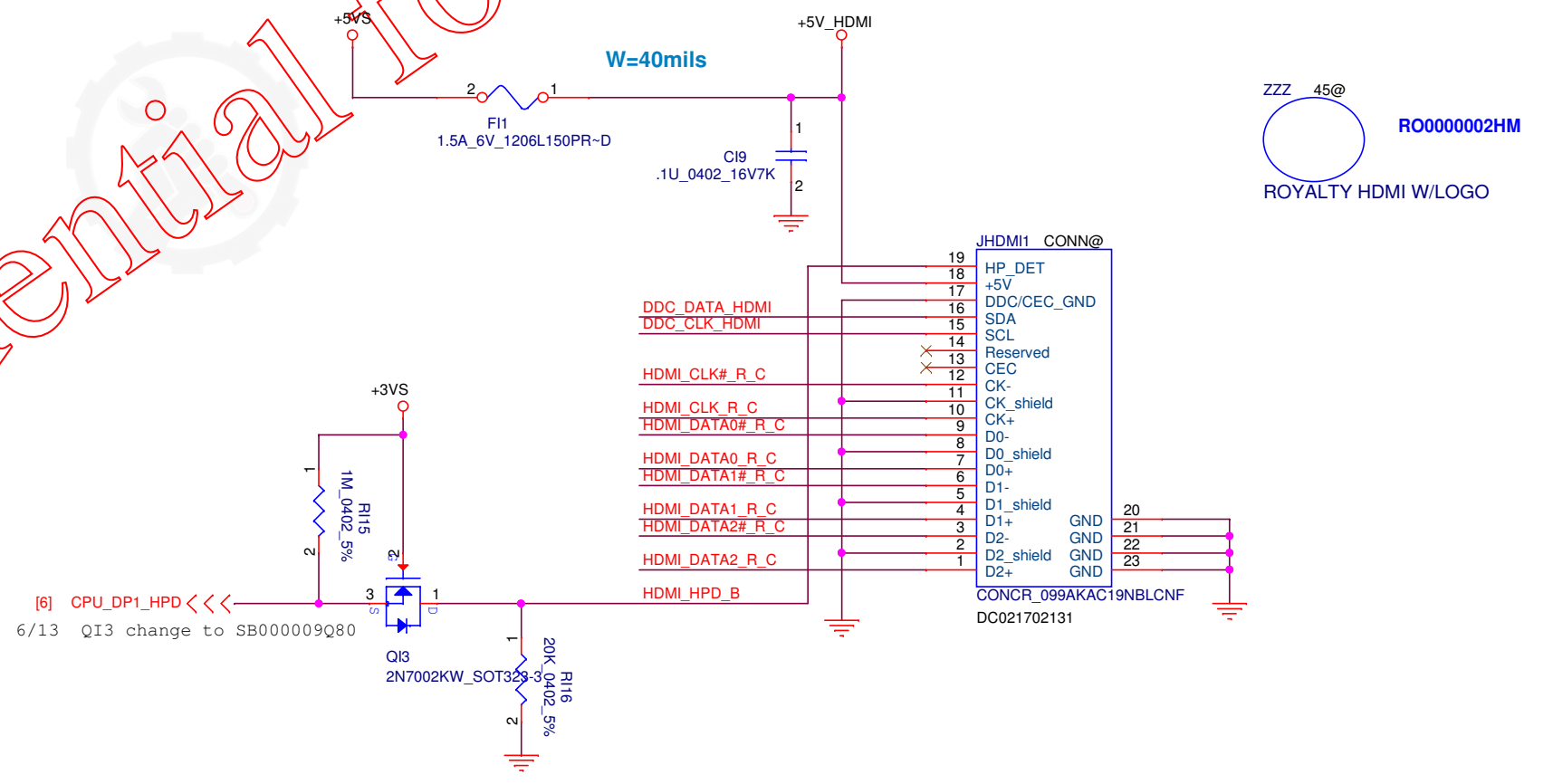
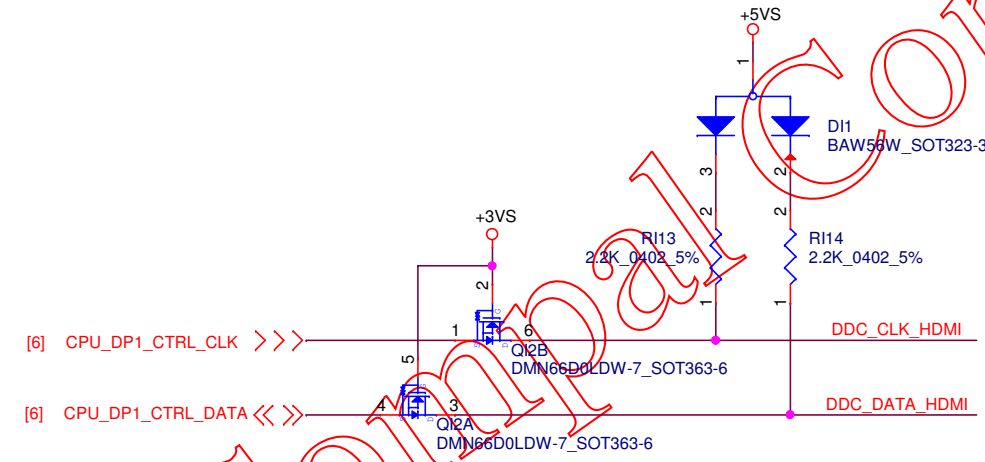
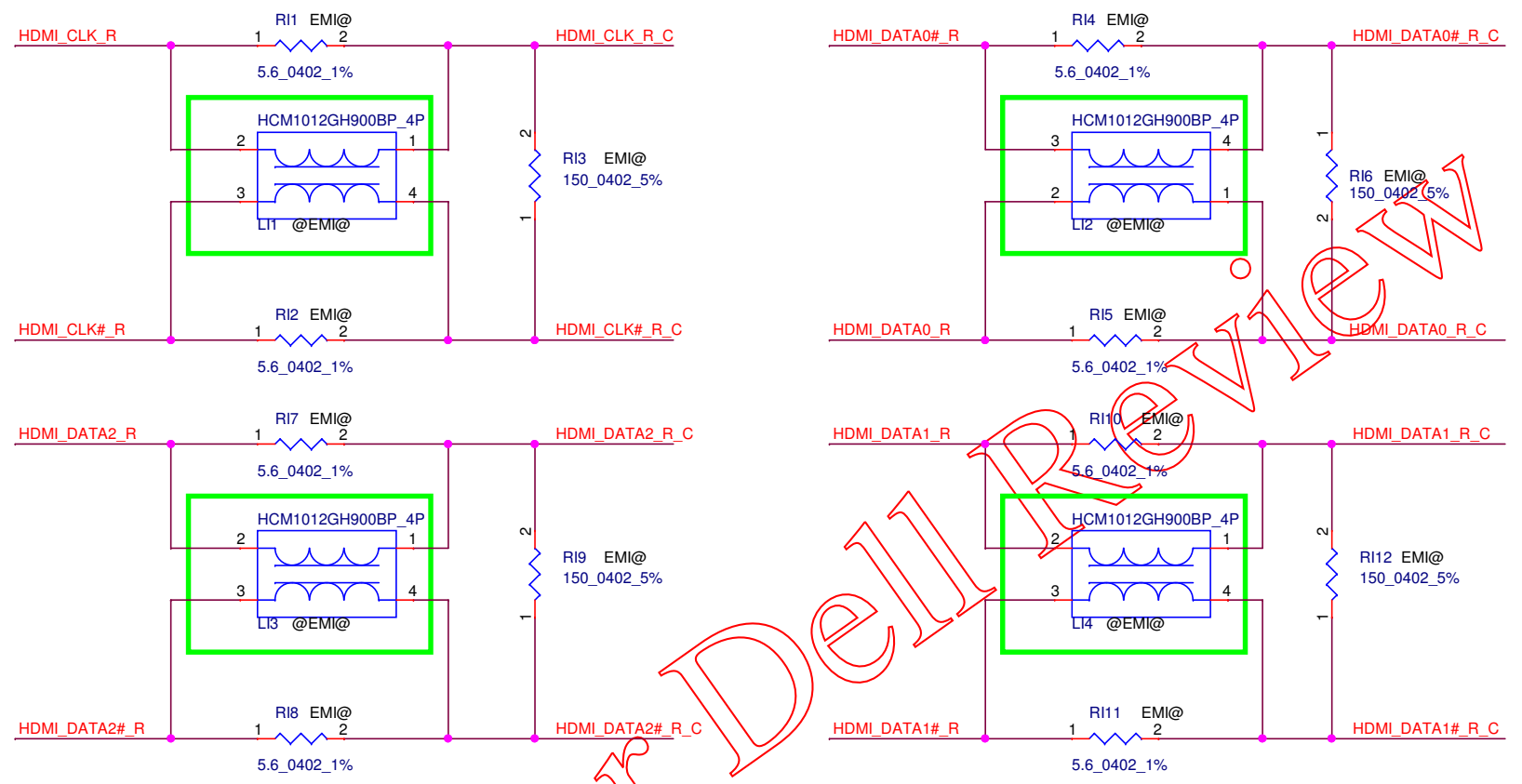
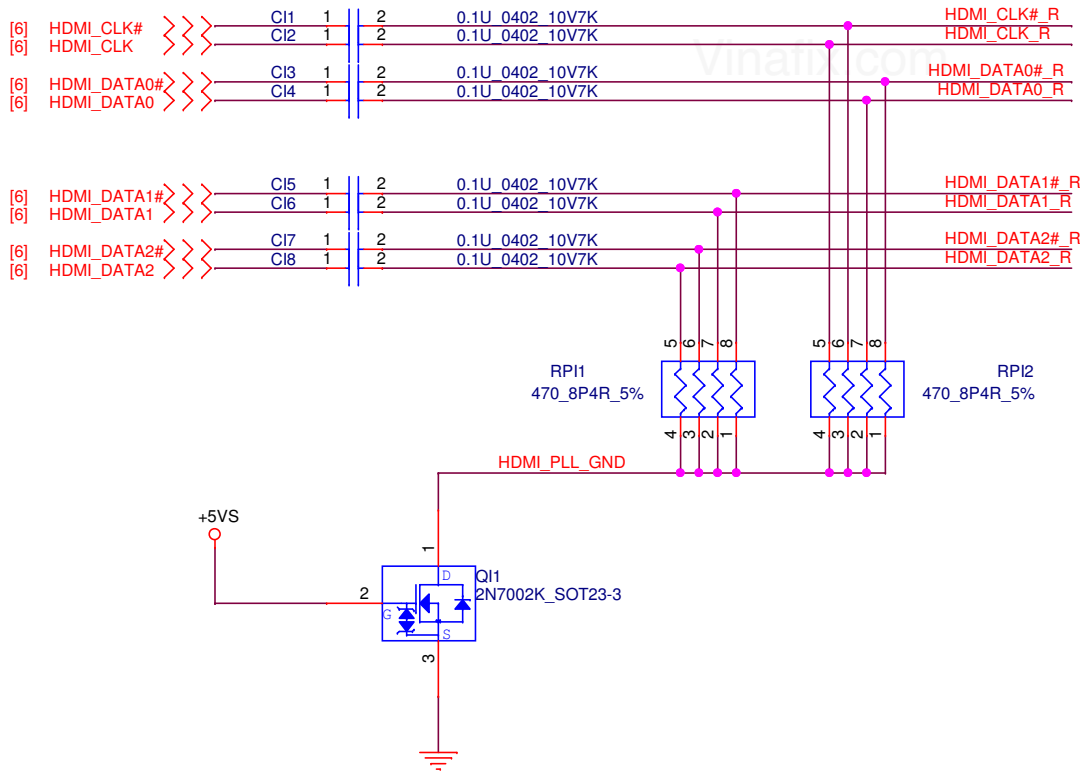
CONN	FFC
GND	S1 1
A+	S2 2
A-	S3 3
GND	S4 4
B-	S5 5
B+	S6 6
GND	S7 7
PRCNT	P1 8
5V	P2 9
5V	P3 10
5V	P3 11
Attention	P4 12
GND	P5
GND	P6

Main Func = WLAN A Key CONN

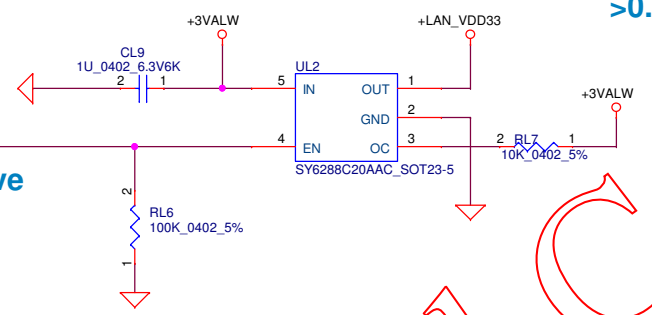
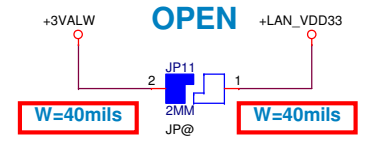
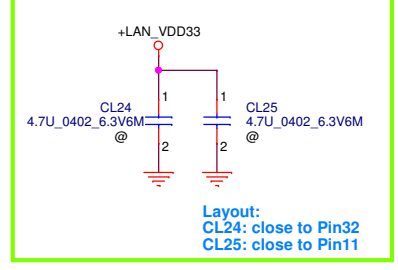
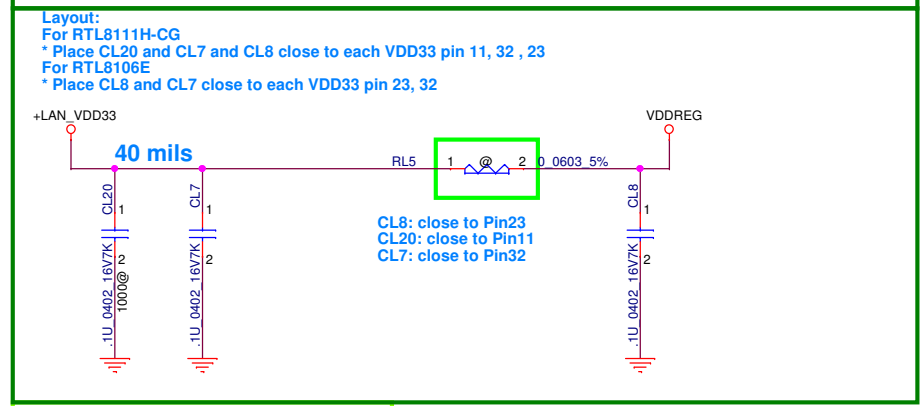
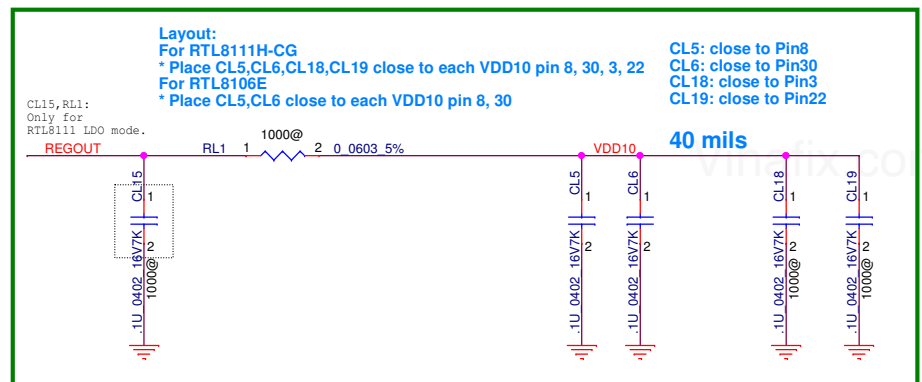


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Size	Document Number	Rev		A00	
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Date:	Wednesday, July 26, 2017	Sheet	32	of	54

Main Func = HDMI



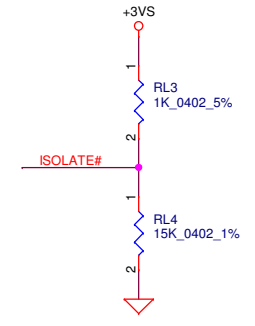
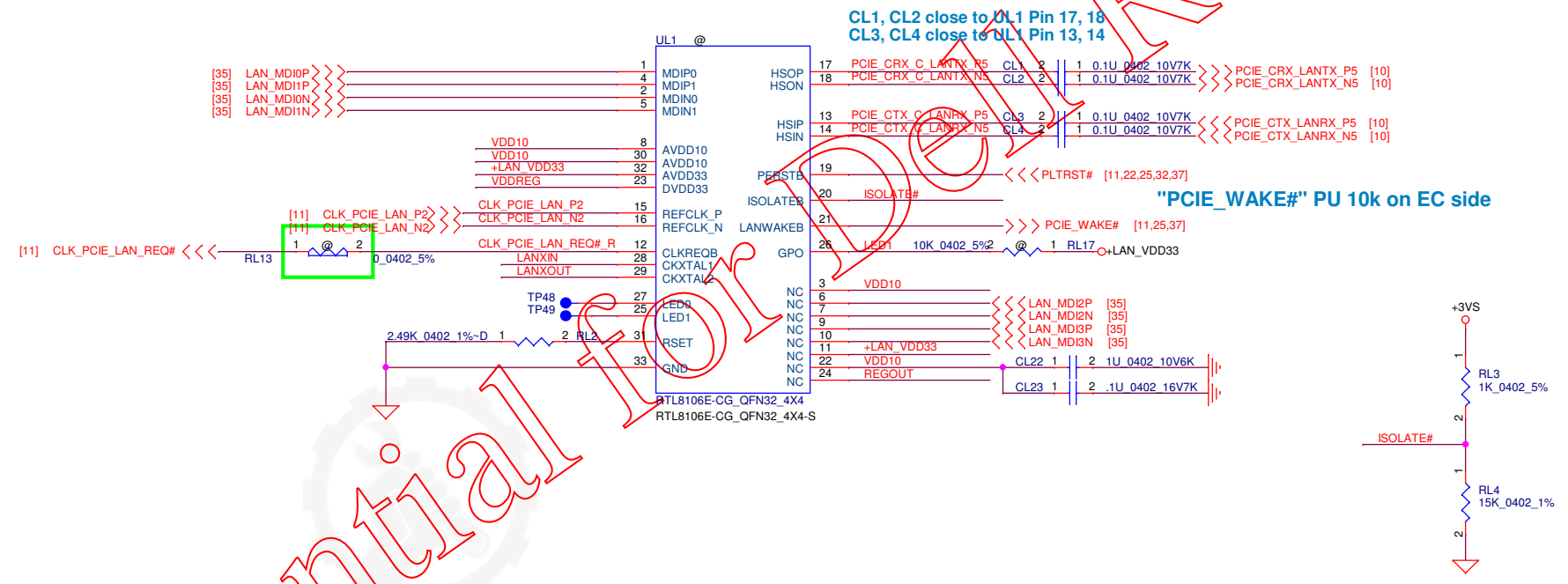
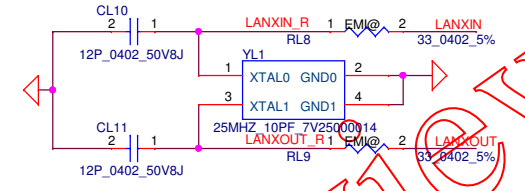
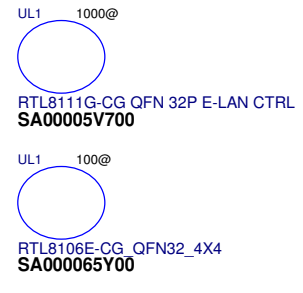
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Issued Date	2016/12/01	Deciphered Date	
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+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.

LAN CHIP 10/100/1000

RTL8111H-CG	RTL8106E-CG
SA000080P00	SA000065Y00
LDO mode	LDO mode
10/100/1000M	10/100M



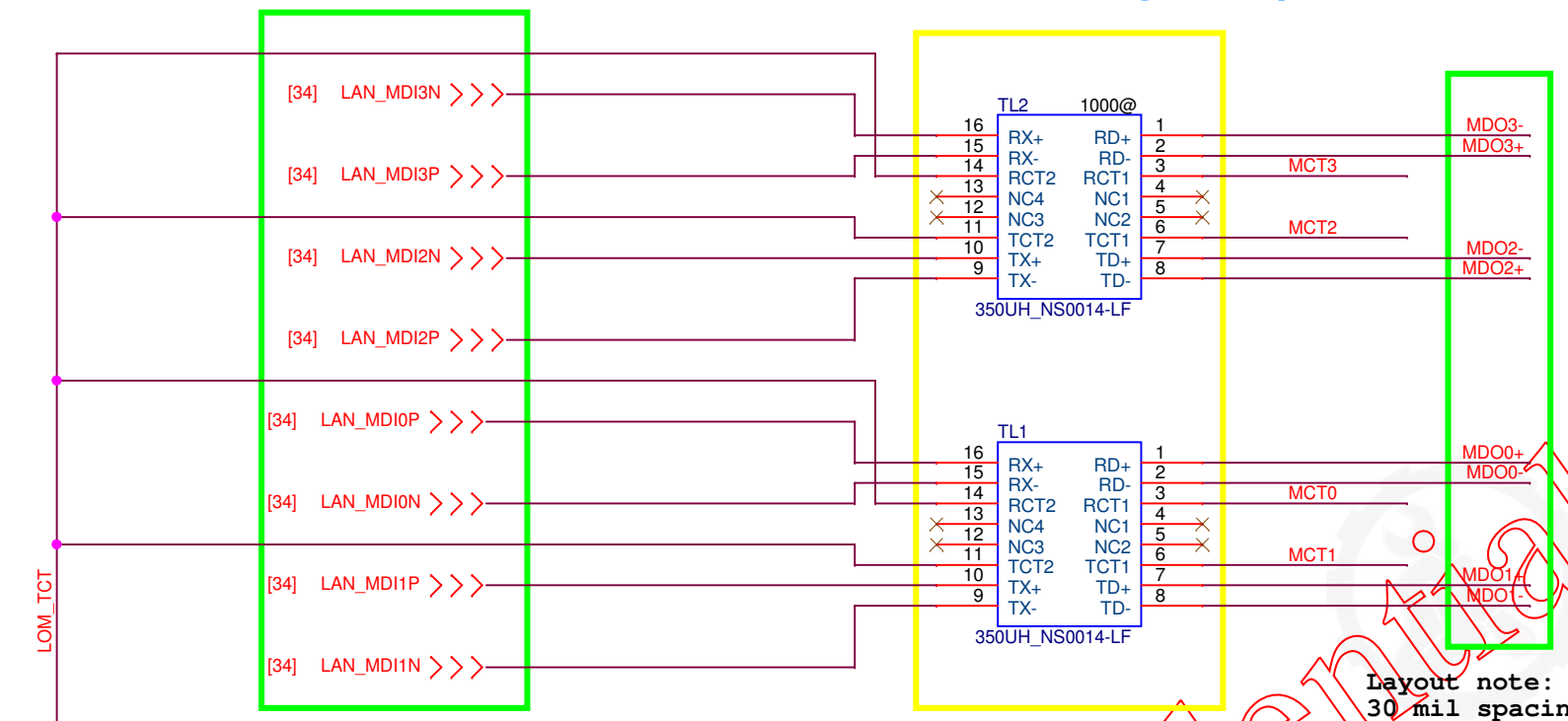
	1.0V Source	RL1	CL15	CL18	CL19	CL20	CL8
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

Confidential

Main Func = LAN LAN Transformer 10/100M x2

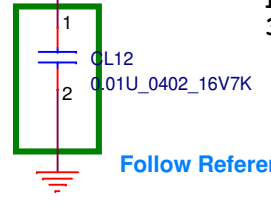
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TL1 TOP, TL2 BOT
2/24 change footprint



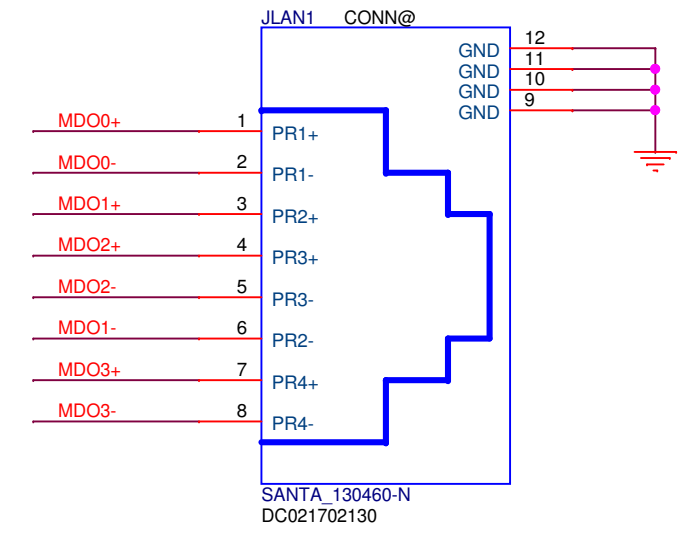
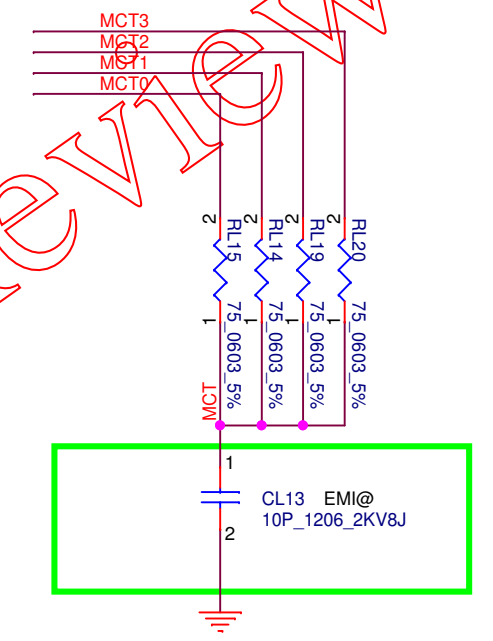
Layout note:
30 mil spacing between MDI differential pairs.

Layout note:
30 mil spacing between MDI differential pairs.



Follow Reference Schematic 0.01uF~0.4uF

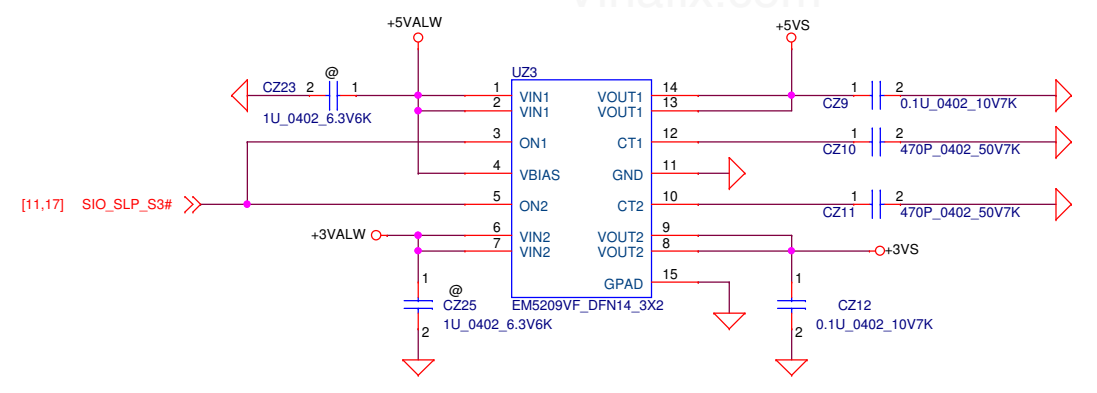
Main: SP050006H00, S X'FORM_ NS0014 LF LAN
2nd: SP050006W00, S X'FORM_ HD-245 10/100 PC CARD LAN



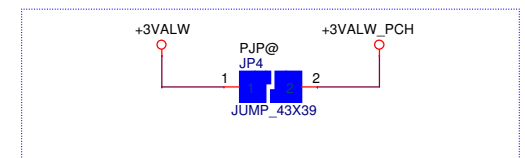
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+5VS/+3VS for System



+3VALW_PCH for System



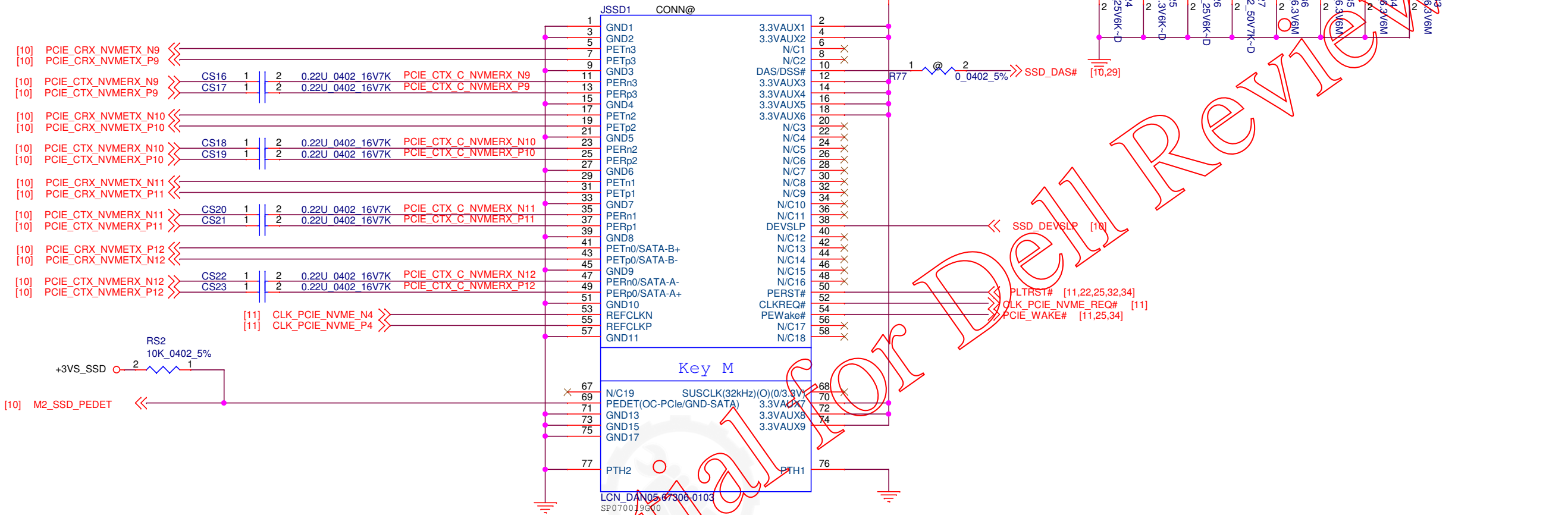
JP4 Short for NON-DS3

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				Custom	LA-F114P
Date: Wednesday, July 26, 2017				Sheet	36 of 54

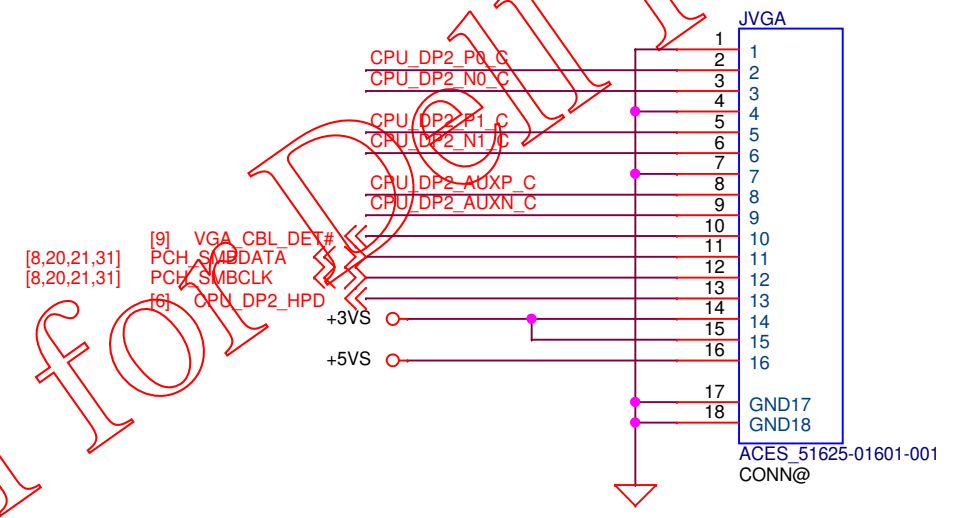
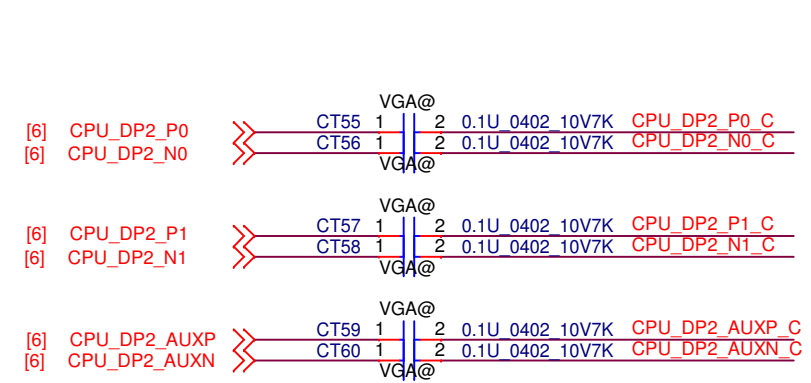
NGFF Key M

JP10 Always Short



PEDET	Module Type
0	SATA
1	PCIE

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VGA CONN

LA-F114P

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				B	LA-F114P	A00	
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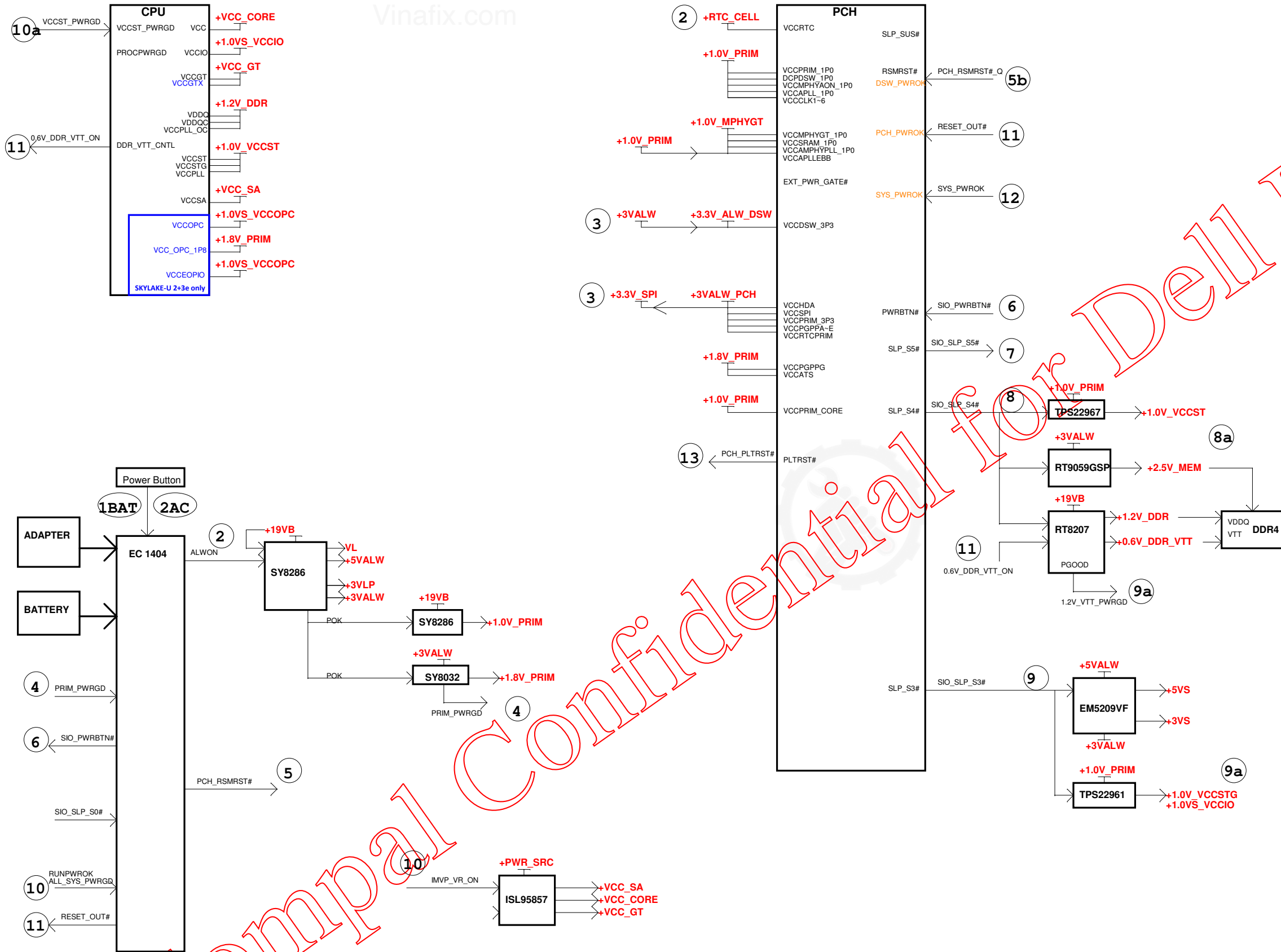
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				B	LA-F114P	A00	
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Timing Diagram for S5 to S0 mode

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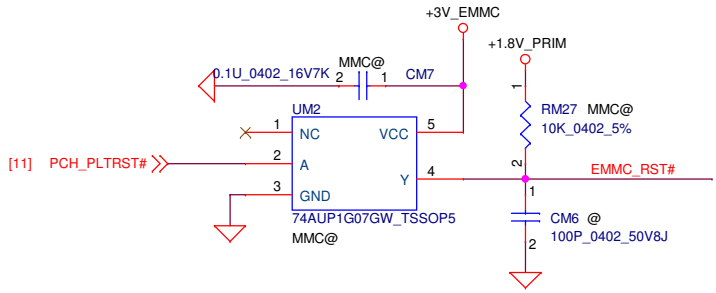
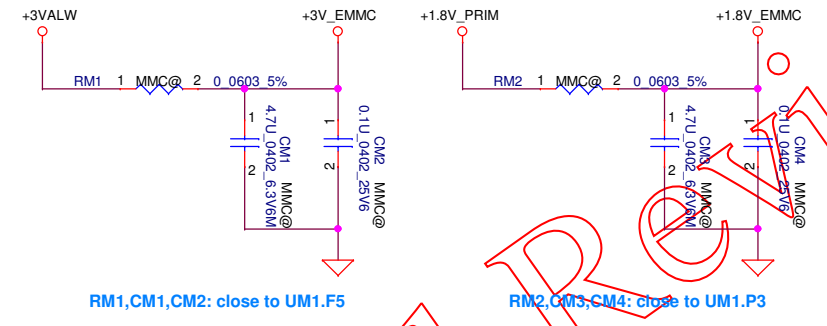
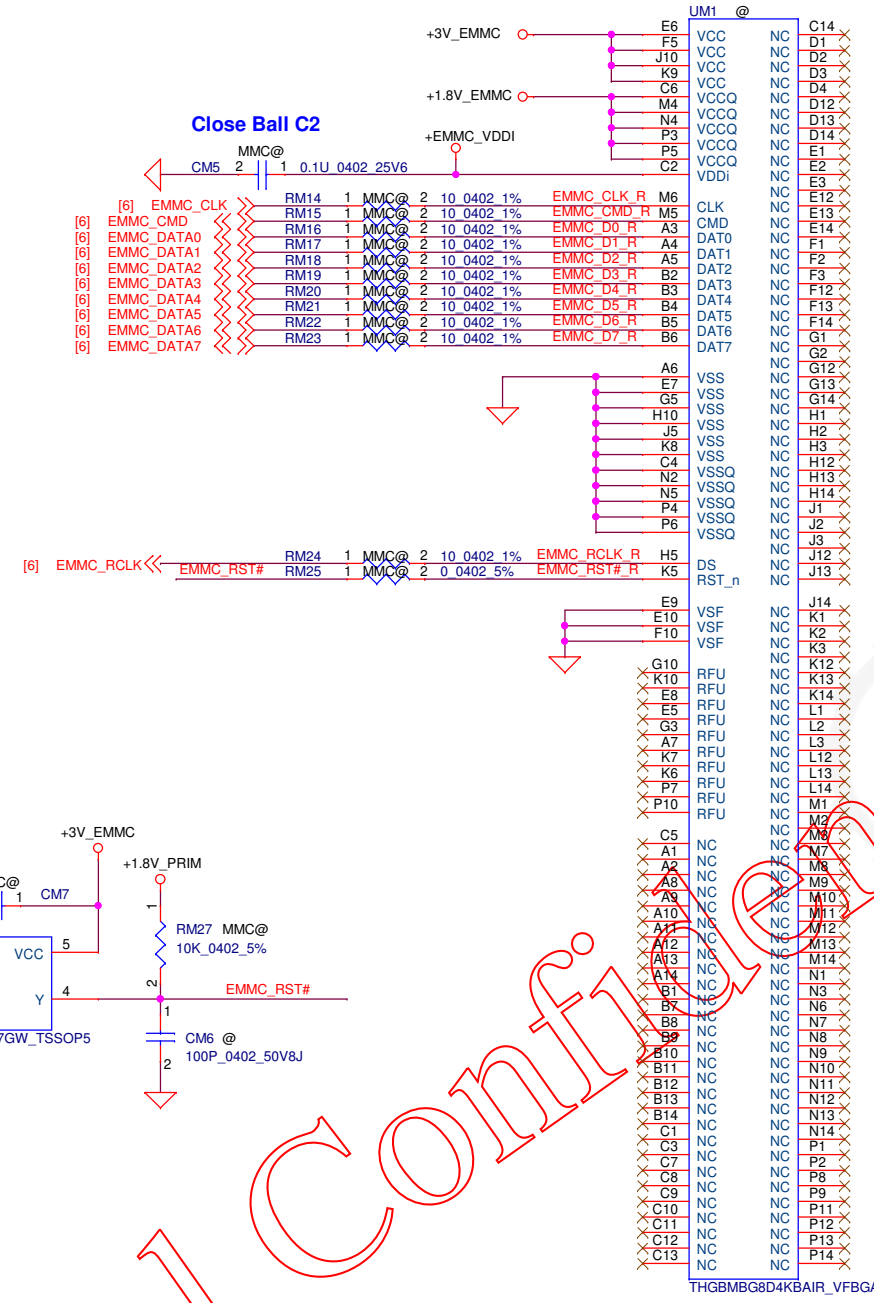
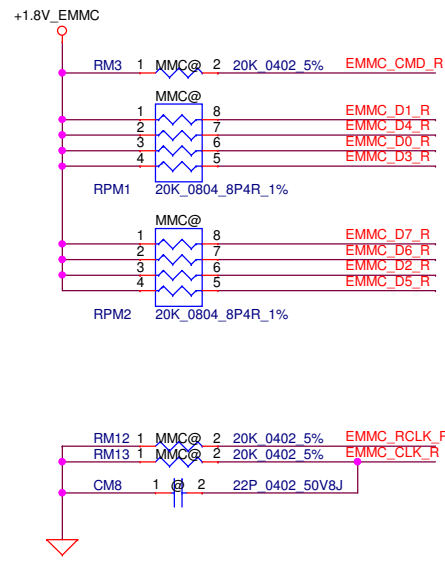


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Main Func = eMMC

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- UM1 SA00009N50L HYNIX HYNIX_128G@ S IC FL 128G H26M88002AMR FBGA 153P
- UM1 SA00009ML0L SANDISK SANDISK_128G@ S IC FL 128G SDINADF4-128G-859 TFBGA

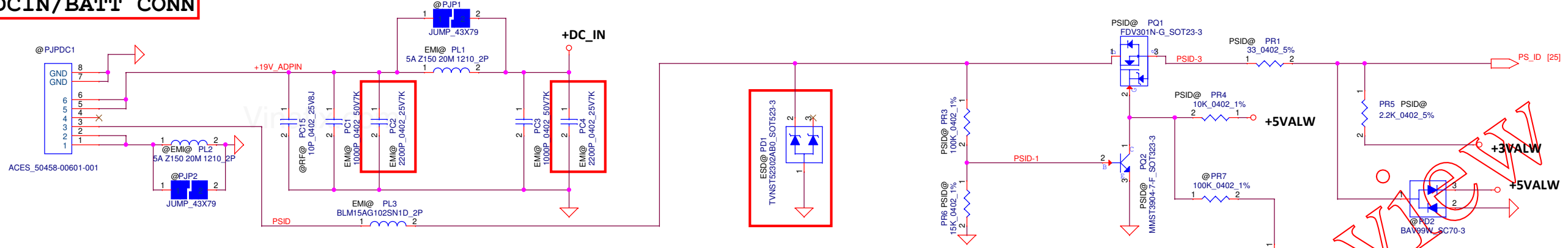
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Size	Document Number	Rev	A00	
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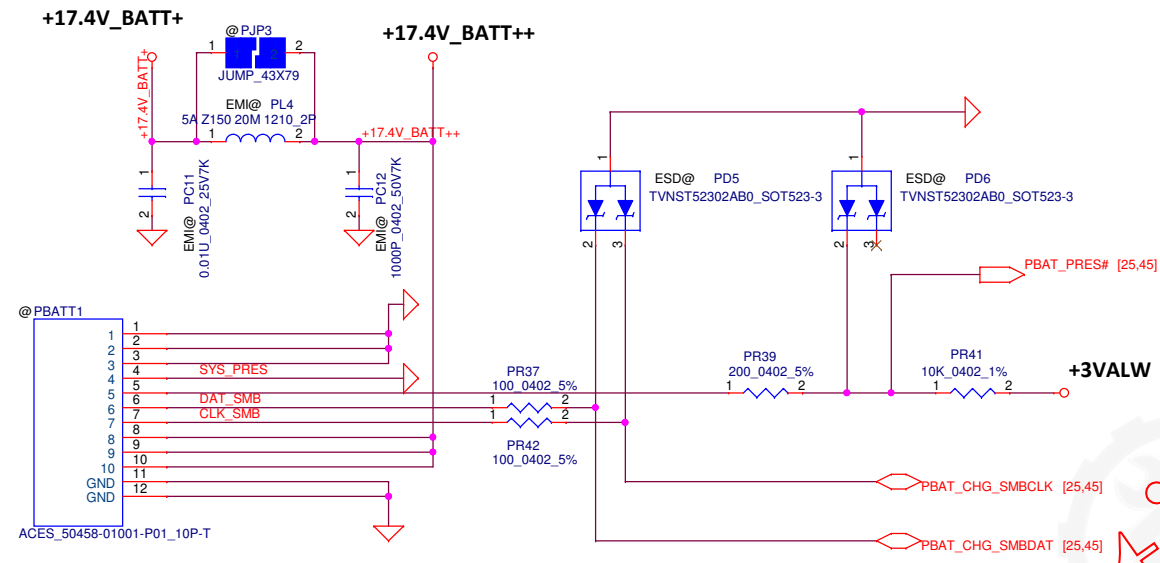
Main Func = DCIN/BATT CONN



Battery Bot Side

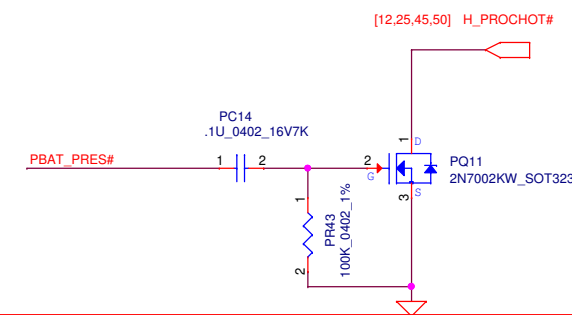
- PIN1 GND
- PIN2 GND
- PIN3 GND
- PIN4 SYS_PRES
- PIN5 BATT_PRS
- PIN6 DAT_SMB
- PIN7 CLK_SMB
- PIN8 Batt+
- PIN9 Batt+
- PIN10 Batt+
- SP021412220

ACES_50458-01001-P01_10P-T



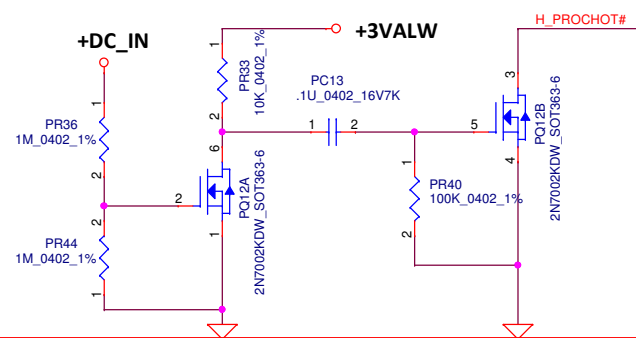
Adapter protection:

if battery removed, adaptor only, then trigger the H_PROCHOT#, keep @ in BOM since battery can not be removed by end user

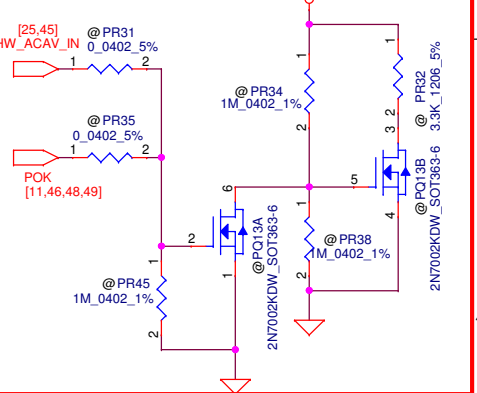


Battery protection:

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW PROCHOT# is issued by EC



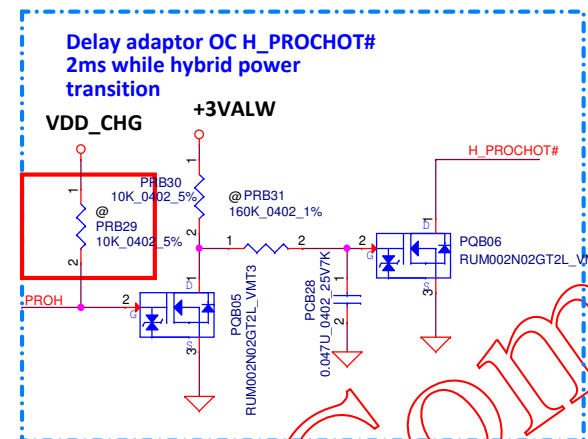
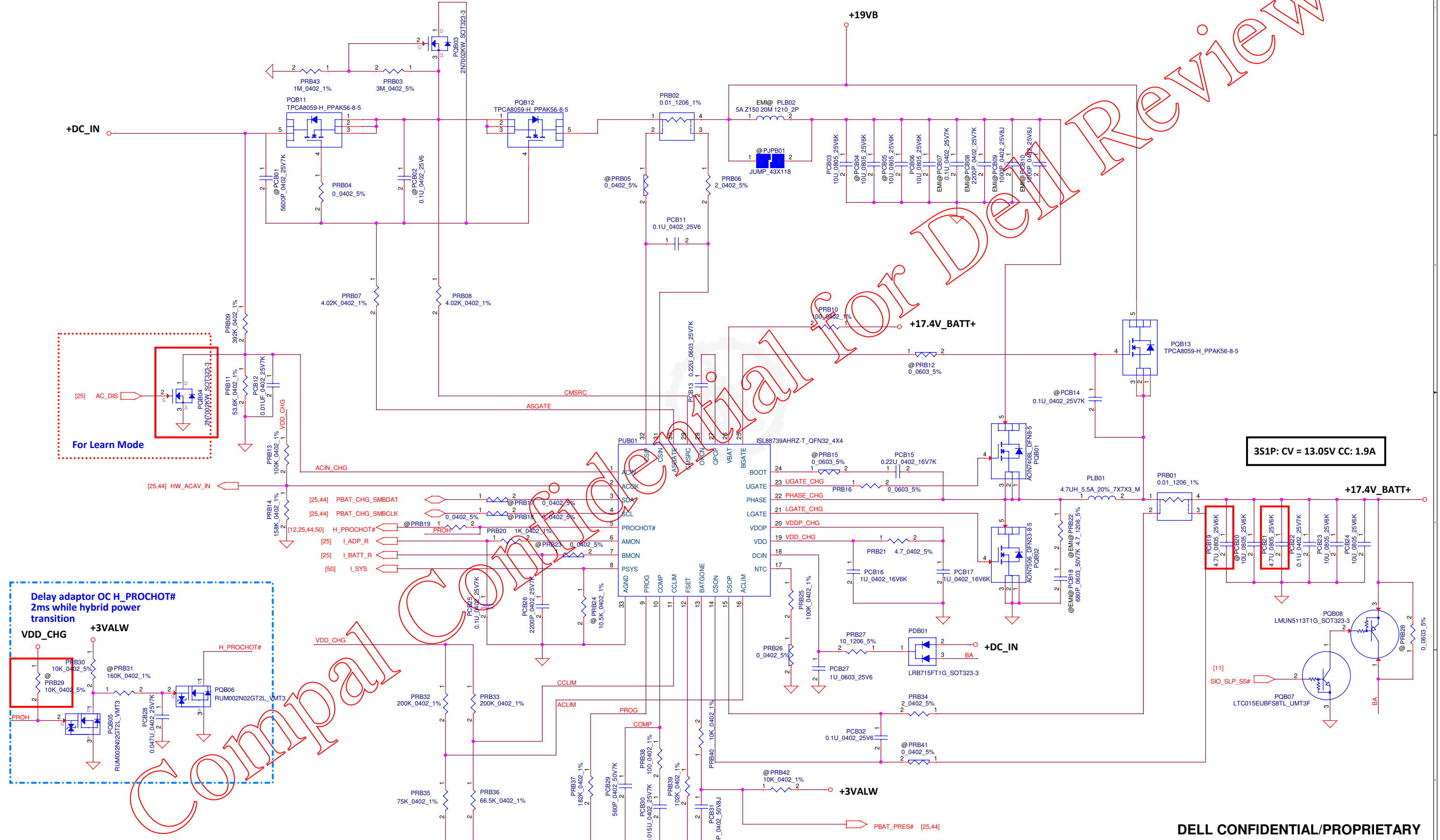
Erp lot6 Circuit



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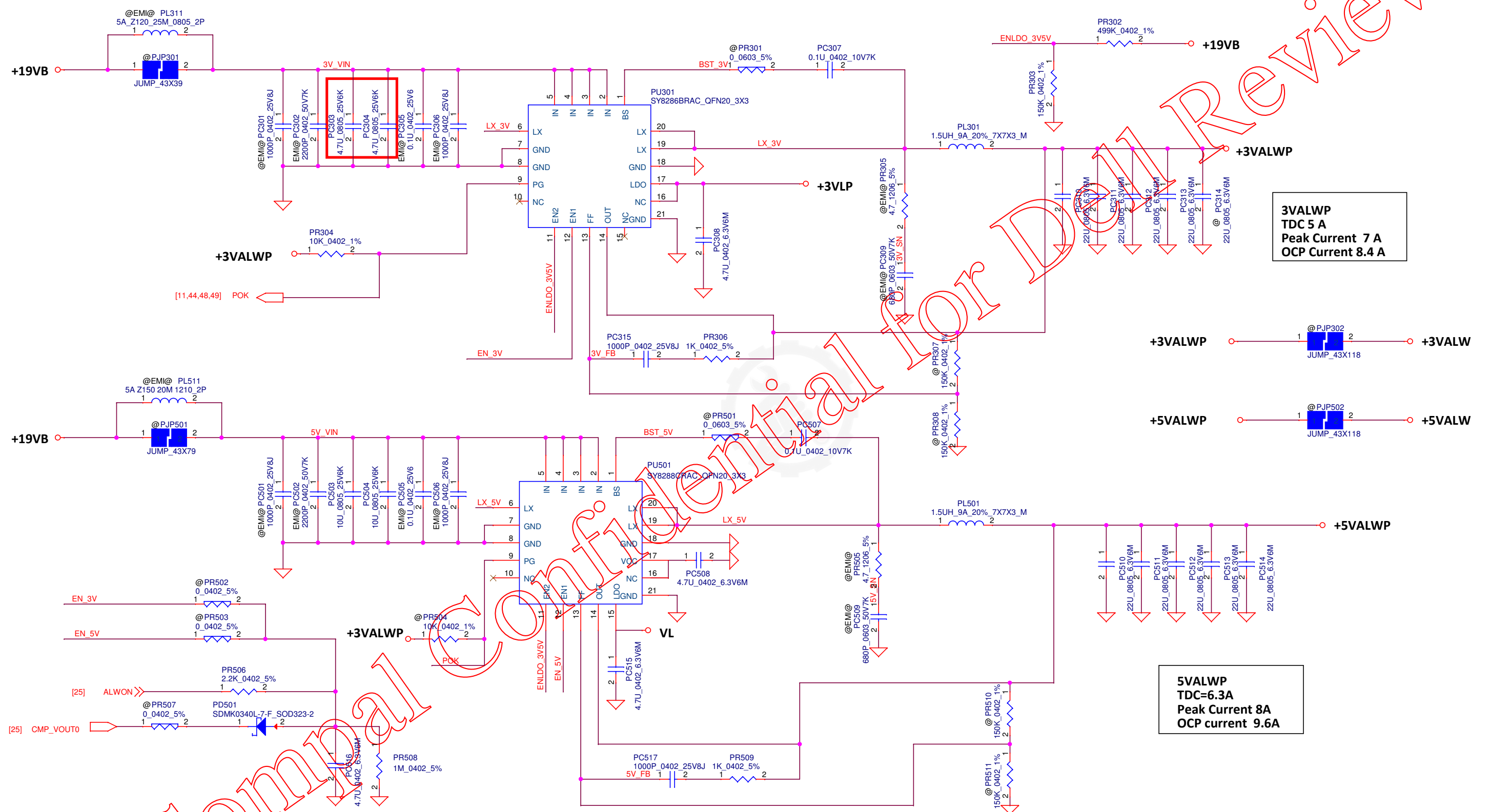
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Main Func = 3.3VALWP/5VALWP

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3VALWP
TDC 5 A
Peak Current 7 A
OCP Current 8.4 A

+3VALWP **+3VALW**

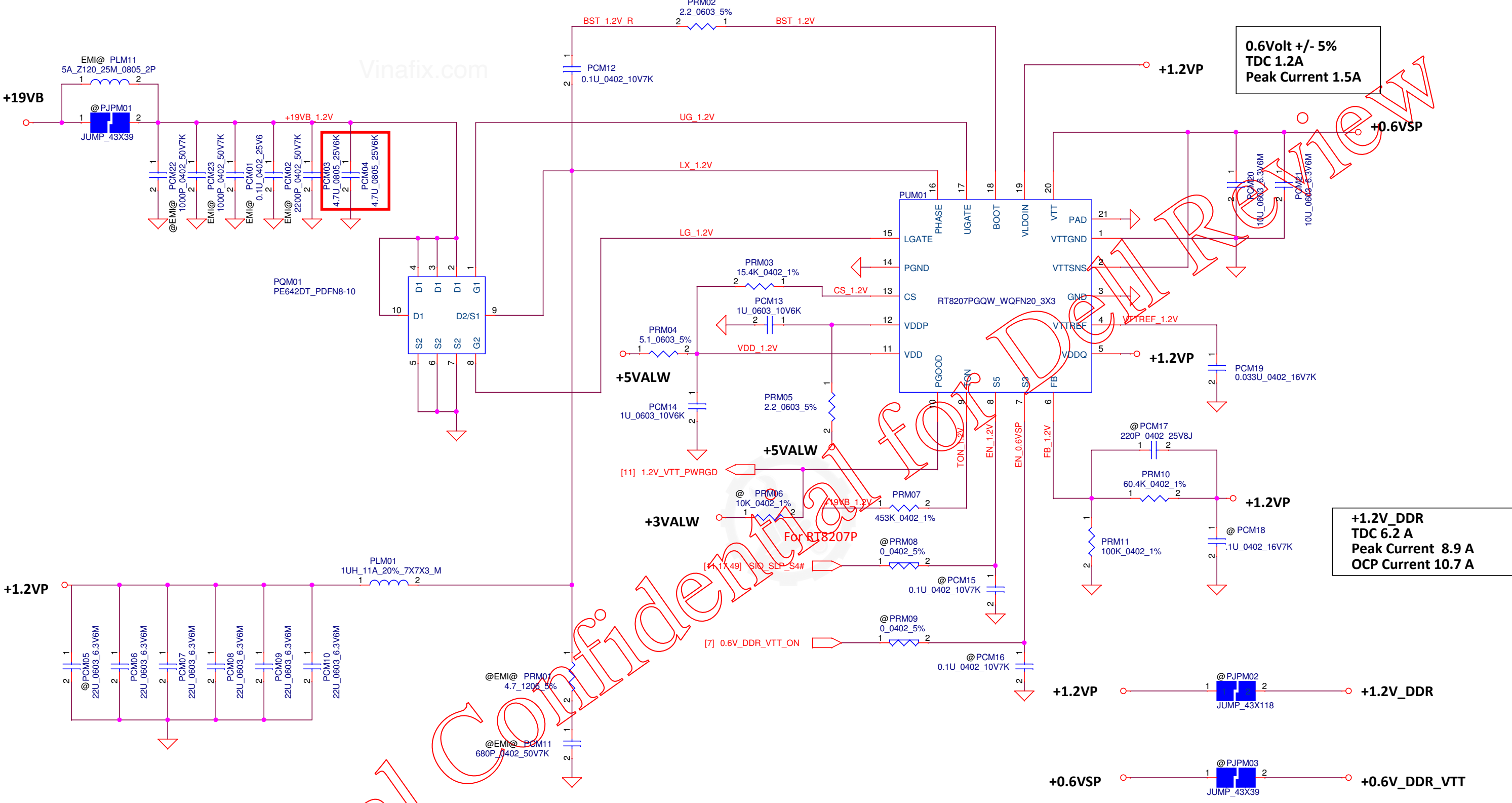
+5VALWP **+5VALW**

5VALWP
TDC=6.3A
Peak Current 8A
OCP current 9.6A

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Date:	Wednesday, July 26, 2017	Sheet	46	of	53

Main Func = +1.2V_DDR/+0.6V_DDR_VTT

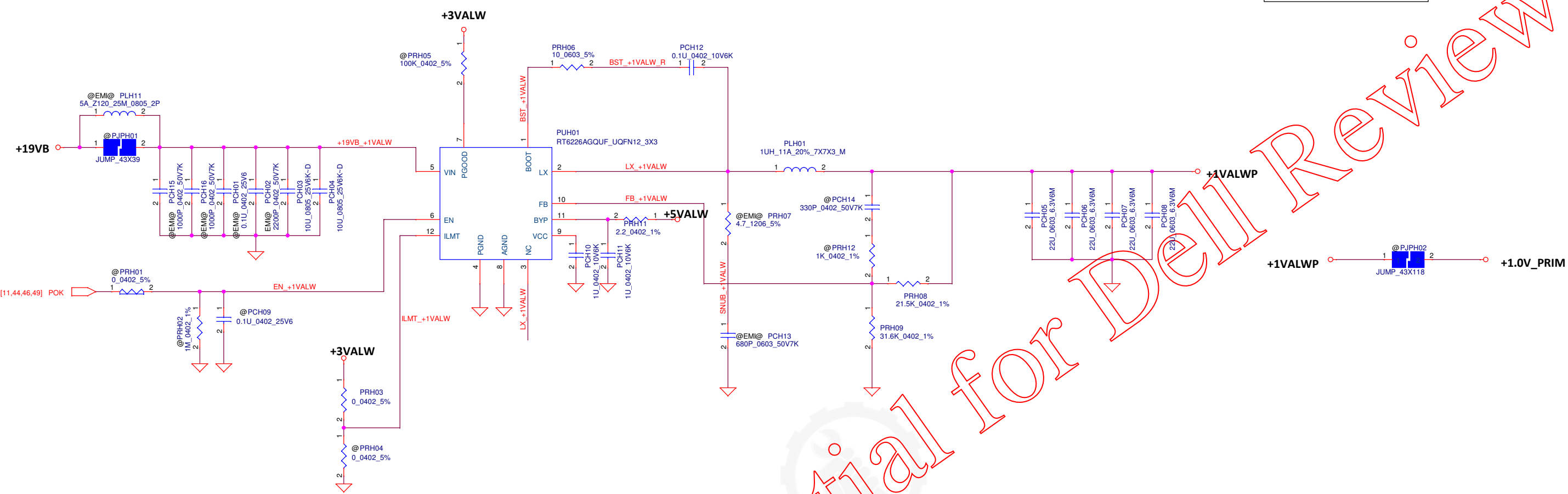


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Main Func = +1VALWP

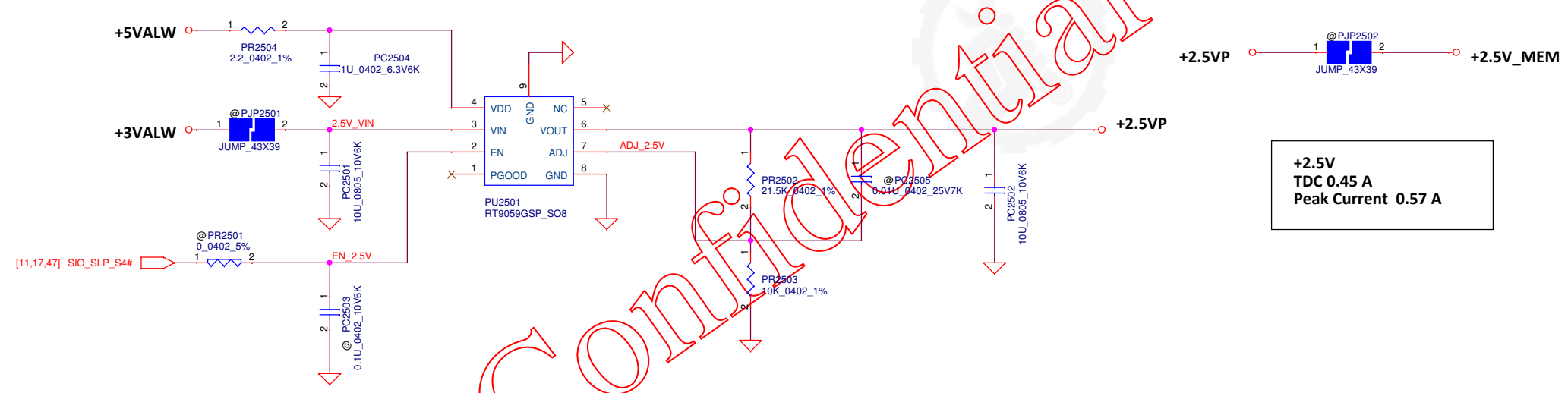
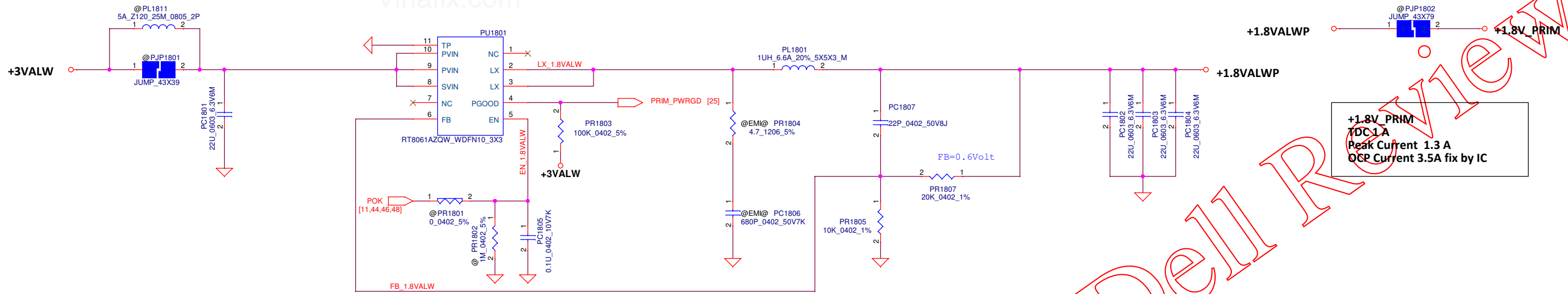
+1.0V_PRIM
TDC 5.2 A
Peak Current 6.5 A
OCP Current 9 A Fix by IC



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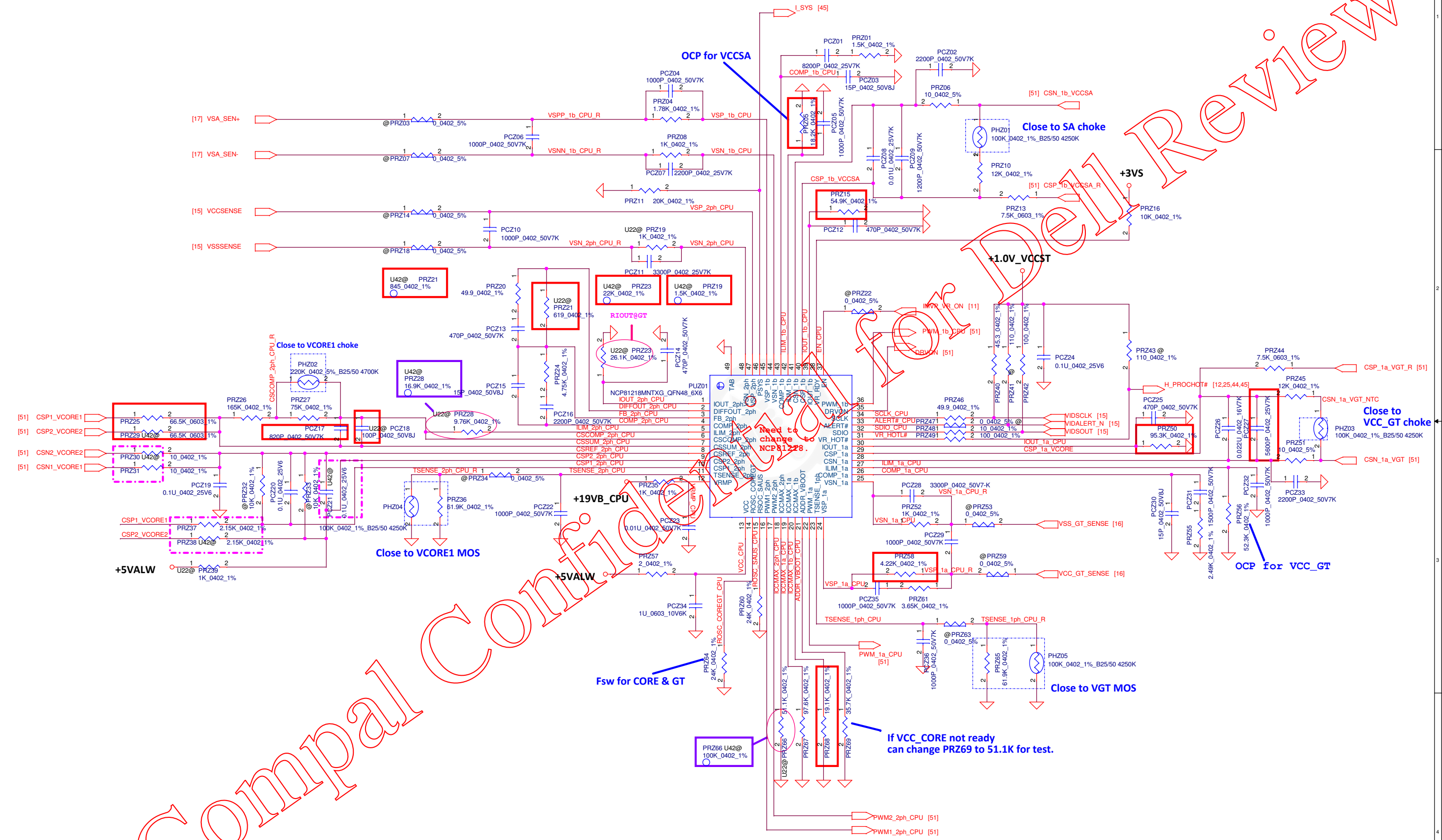
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Main Func = +1.8VALWP / +2.5VP



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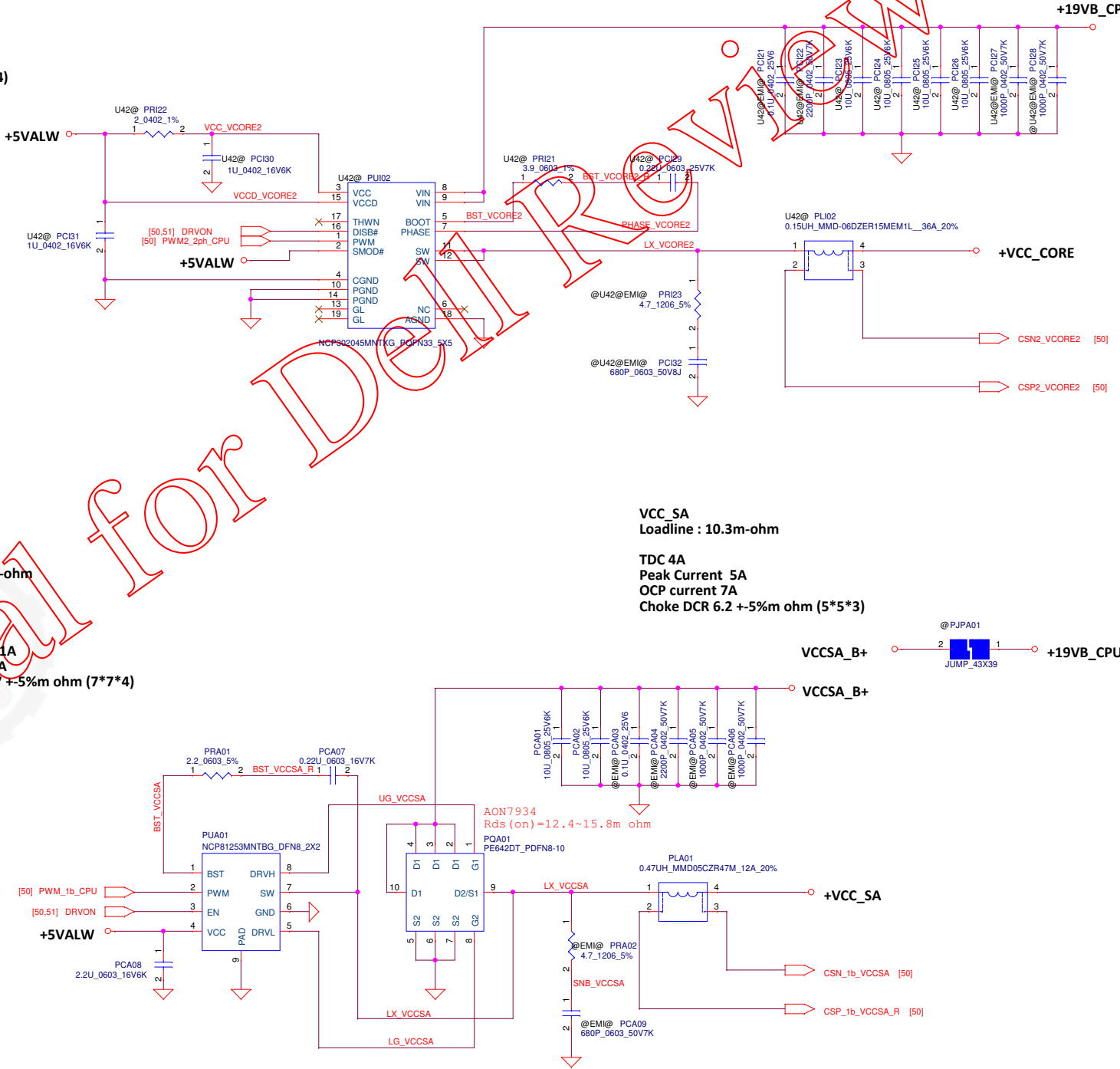
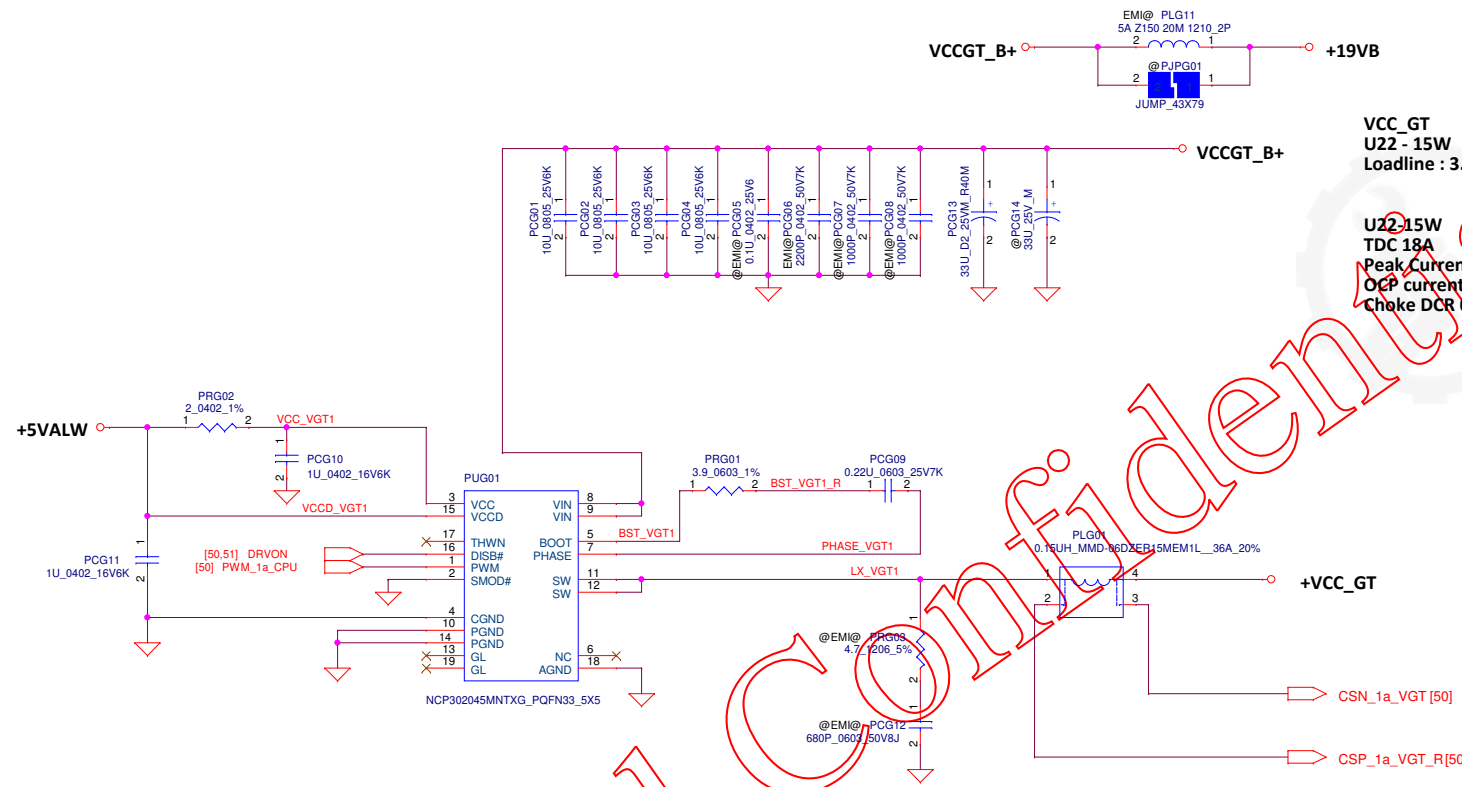
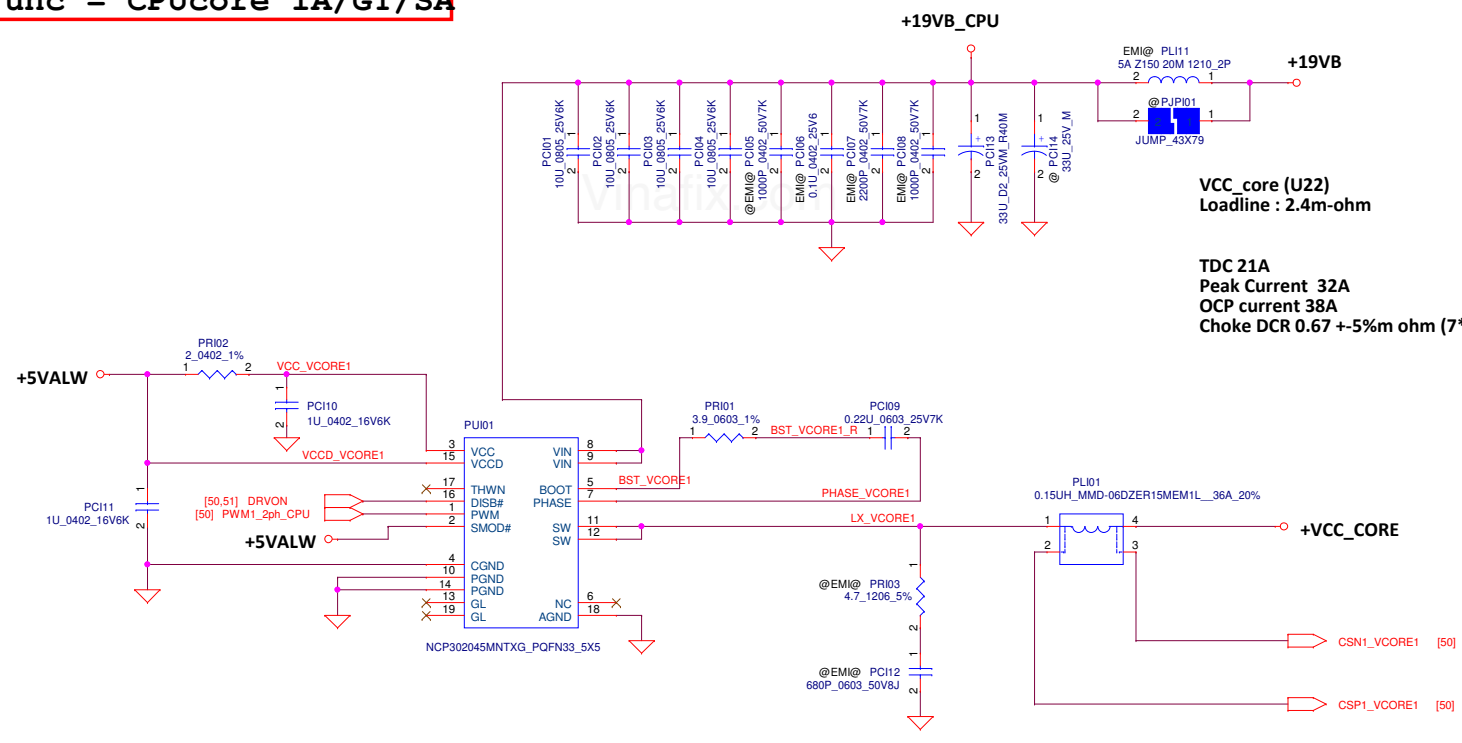
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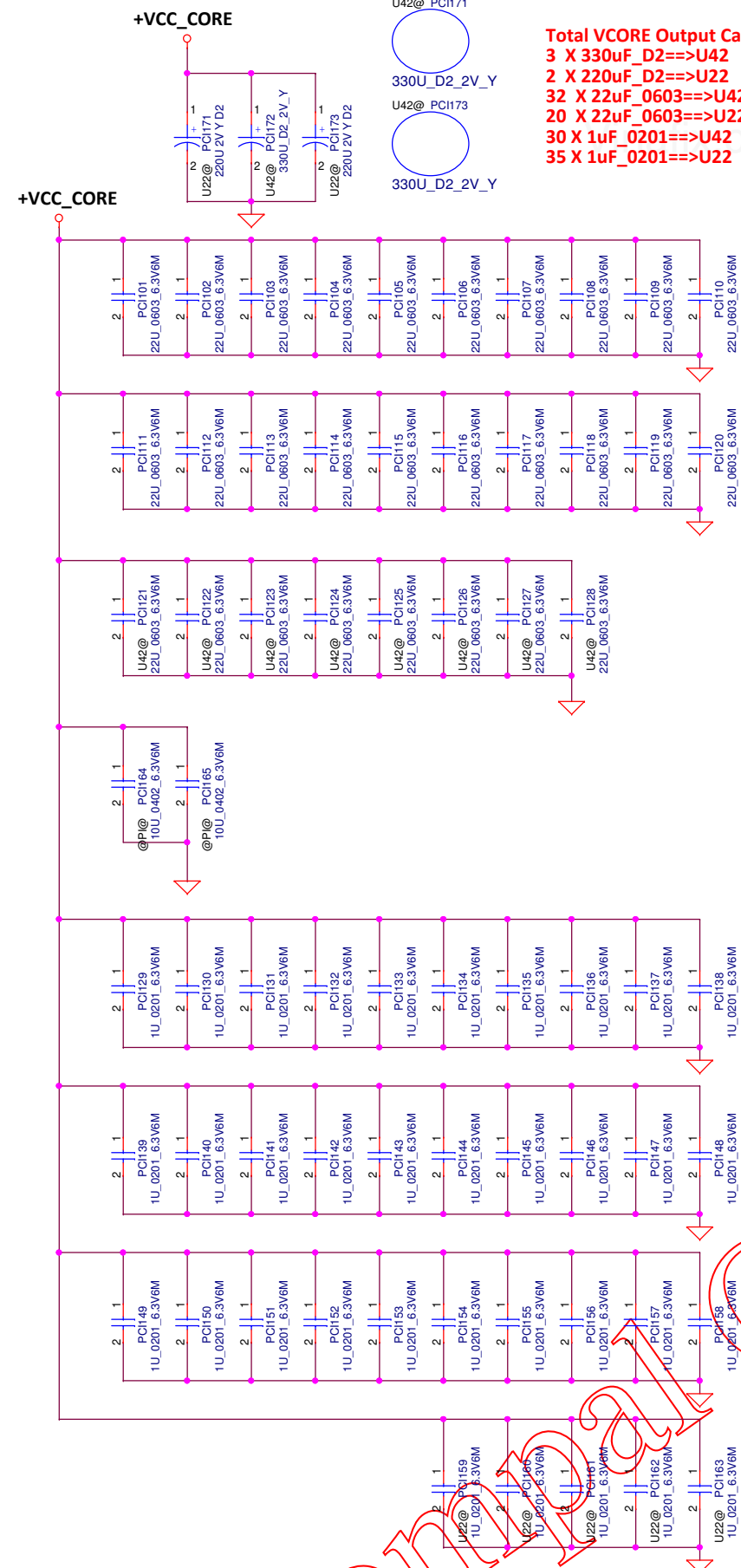
Main Func = CPUcore IA/GT/SA



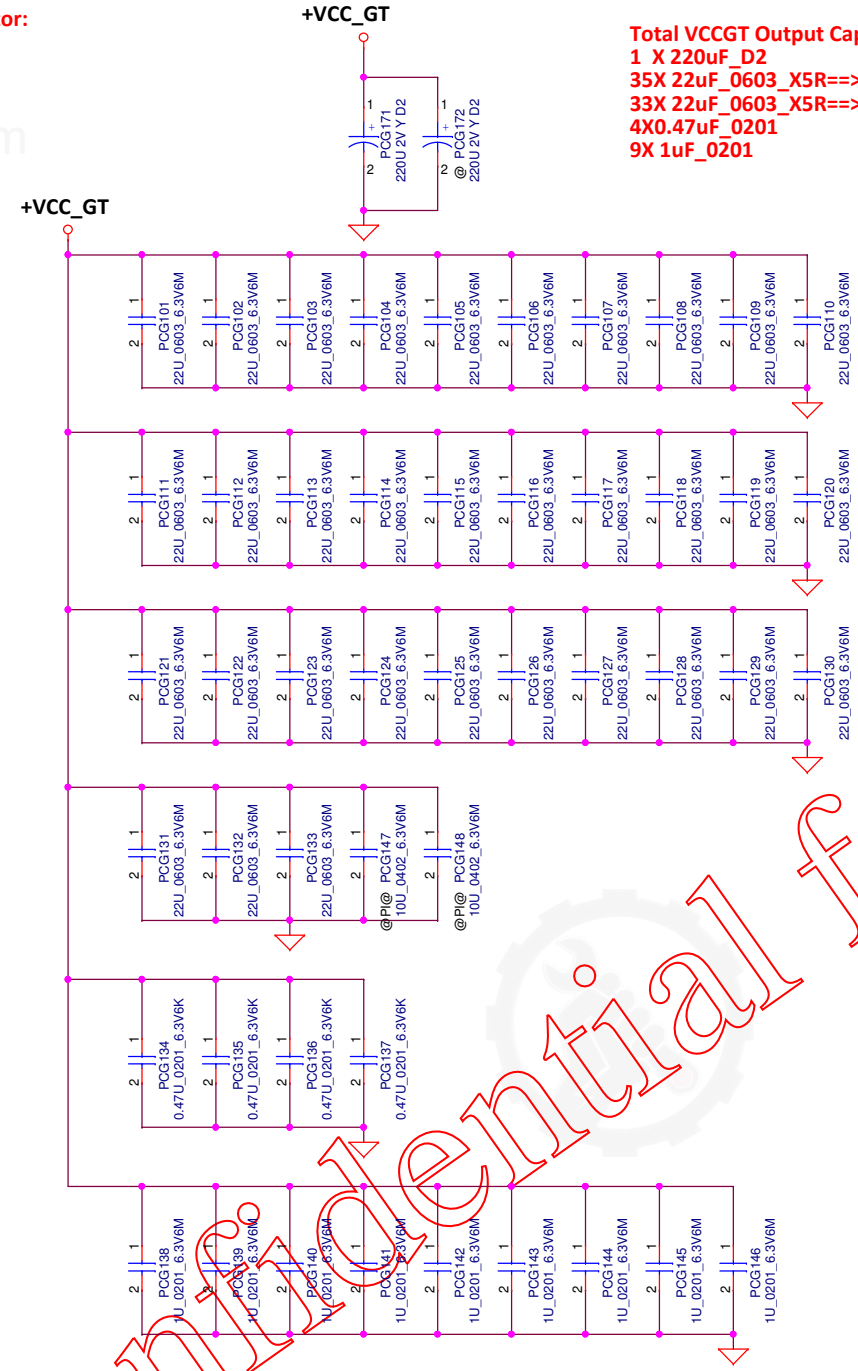
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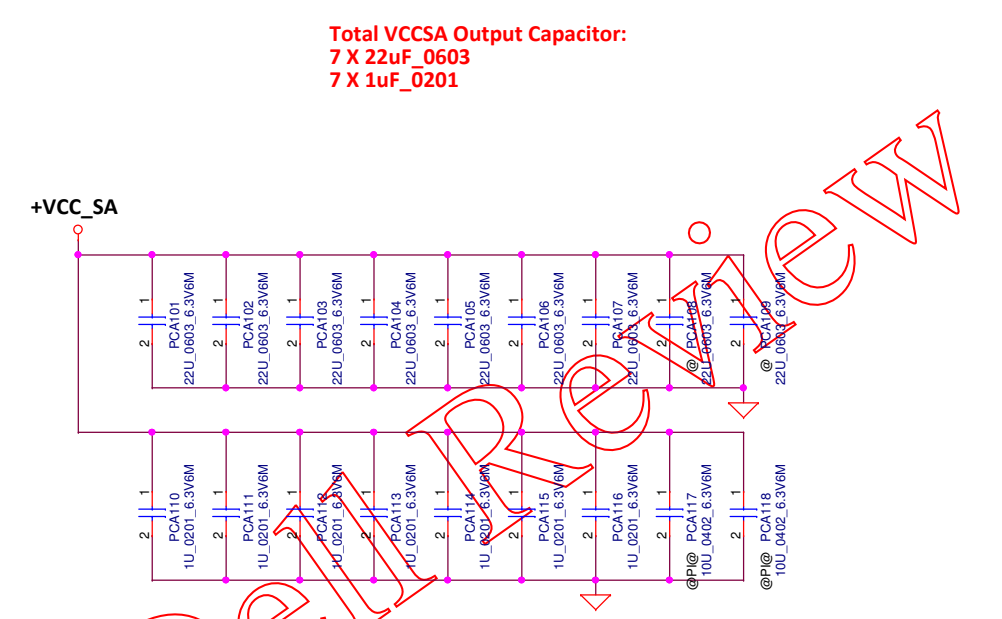
Main Func = CPU/ VGA / SA MLCC



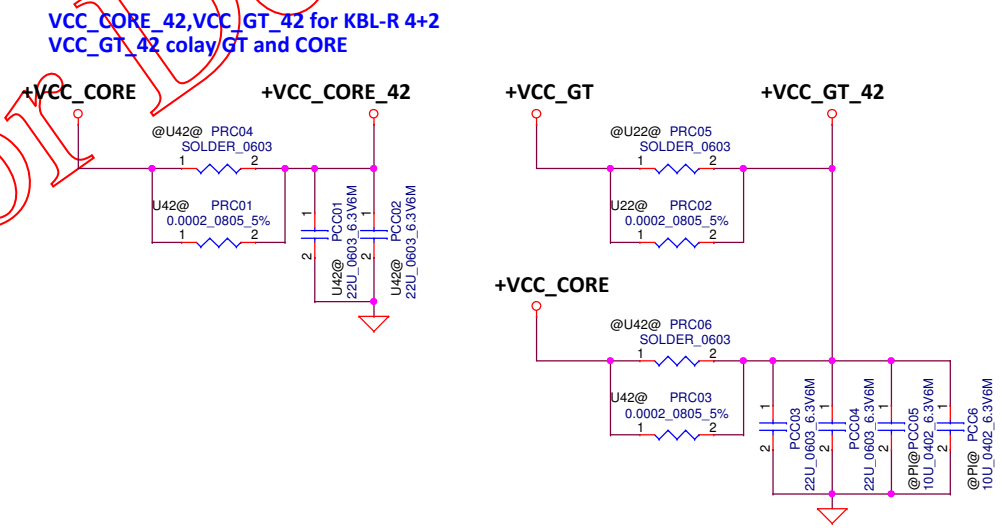
Total VCORE Output Capacitor:
 3 X 330uF_D2==>U42
 2 X 220uF_D2==>U22
 32 X 22uF_0603==>U42
 20 X 22uF_0603==>U22
 30 X 1uF_0201==>U42
 35 X 1uF_0201==>U22



Total VCCGT Output Capacitor:
 1 X 220uF_D2
 35X 22uF_0603_X5R==>U22
 33X 22uF_0603_X5R==>U42
 4X0.47uF_0201
 9X 1uF_0201



Total VCCSA Output Capacitor:
 7 X 22uF_0603
 7 X 1uF_0201



VCC_CORE_42, VCC_GT_42 for KBL-R 4+2
 VCC_GT_42 colay GT and CORE

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8							

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