COMPAL CONFIDENTIAL

MODEL NAME : Loki15/17

PCB NO : DA8001BS000

BOM P/N : 431A7Y31L01

KBL-U+MEC1416 board

2017-07-28

REV : 1.0 (A00)

PCB R1	PCB R3
ZZZ DA8001BS000 PCB@ PCB 21C LA-F115P REV0 M/B 3	ZZZ DAZ21C00101 PCB_R3@ PCB CAL50 LA-F115P LS-F111P GOLD A31 !

KBL R1	KBL R3
UC1 SA0000AWC0L i7KBLR_1.8G_QS@ S IC A31 FJ8067703281816 QNBF Y0 1.8G	UC1 SA0000AWC2L i7KBLR_R3@ S IC FJ8067703281816 SR3LC Y0 1.8G A31!
UC1 SA0000A370L i5KBLU_2.5G_R1@ S IC FJ8067702739739 SR2ZU H0 2.5G A31!	UC1 SA0000AWB3L i5KBLR_R3@ S IC FJ8067703282221 SR3LB Y0 1.6G A31!
UC1 SA0000AWB1L i5KBLR_1.6G_QS@ S IC A31 FJ8067703282221 QNEG Y0 1.6G	UC1 SA0000B2Y1L i3KBLU_R3@ S IC FJ8067702739765 SR3JY H0 2.7G A31!
UC1 SA0000AQZ0L i7KBLR_1.8G_ES@ S IC A31 FJ8067703281813 QN5C Y0 1.8G	UC1 SA0000ADV3L KBLU_Pentium_R3@ S IC FJ8067702739932 SR348 H0 2.3G A31!
UC1 SA0000A344L i7KBLU_2.7G@ S IC FJ8067702739740 SR2ZV H0 2.7G A31!	UC1 SA0000ADL3L KBLU_Celeron_R3@ S IC FJ8067702739933 SR349 H0 1.8G A31!
UC1 SA0000ACL0L i3SKL_2.0G_SMB0@ S IC FJ8066201931106 SR2UW D1 2G A31!	UC1 SA0000ACL1L i3SKL_SMB0_R3@ S IC FJ8066201931106 SR2UW D1 2G A31!

@ : Un-pop Component
UMA@/DIS@ : UMA & DIS Type
U22@/U42@ : KBL U/KBL U-R
SKL@/KBL@:SKL/KBL
EC@ : EC
JP@/PJP@ : JUMP

EMI@/ESD@/RF@ : EMI, ESD and RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component
TYPEC@EMI@/TYPEC@ESD@/TYPEC@RF@:EMI, ESD ,RFTYPEC Component
MAD@RF@:RF MAD Component
LOKI@EMI@/LOKI@ESD@:EMI/ESD LOKI Component
CMC@ : XDP Component
CONN@ : Connector Component
TP_WAKE@/NTP_WAKE@ : TouchPad wake
KBBL@ : KB Backlight
TPM@/FTPM@ : HW TPM/SW TPM
MMC@ : eMMC
FFS@ : Free Fall Sensor
TYPEC@/LOKI@TYPEC@ : typeC
DSX@ : Deep sleep
GEN8@/GEN9@:RTC GEN8/9
ODD@:ODD Component
FP@:Finger Printer

M2_50@ : GPU R17M_2_50
2G@/2G_H@/2G_S@/2G_M@ : VRAM type
4G@/4G_H@/4G_S@/4G_M@ : VRAM type

Layout Dell logo

REV: X00
PWB: 9HTP8

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

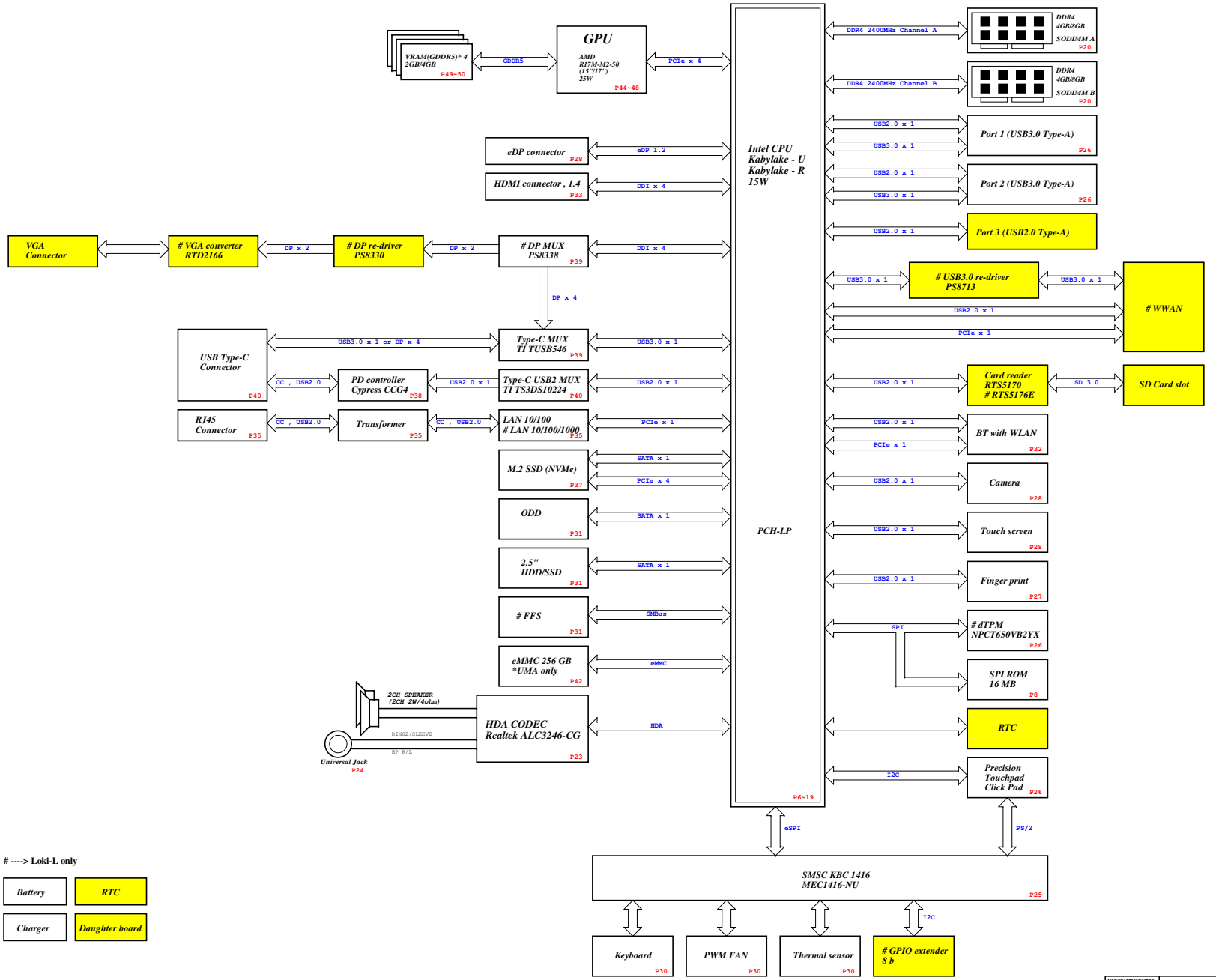
Compal Electronics, Inc.

Title: Cover Page

Size | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 1 of 65

Loki/Loki-L Block Diagram



----> Loki-L only

Battery	RTC
Charger	Daughter board

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: Block Diagram

Size: Document Number: LA-F115P

Rev: 0.1

Date: Friday, July 06, 2017 Sheet 3 of 65

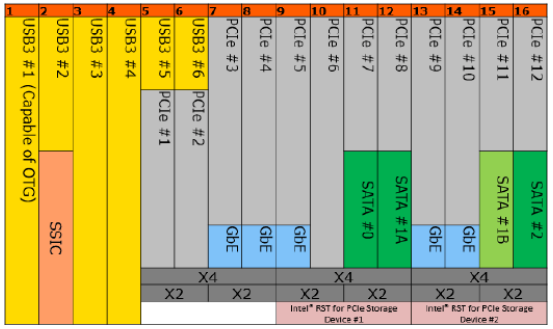
POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	LOW	HIGH	HIGH	ON	ON	OFF	OFF

Voltage Rails

Power Plane	Description	S0	S3	DS3	S4/S5	M3
+SDC_IN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+1.0V_PRIM	System +1.0V power rail	ON	ON	OFF	ON*	ON
+1.0VS_VCCIO	+1.0VS IO power rail	ON	OFF	OFF	OFF	OFF
+1.0V_MPHYPLL	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	OFF	ON/OFF	ON
+0.95VSDGPU	+0.9VS power rail for GPU	ON	OFF	OFF	OFF	ON
+1.35V_MEM_GFX	+1.35VS power rail for GPU	ON	OFF	OFF	OFF	ON
+1.2V_DDR	DDR4/L-RS +1.2V power rail	ON	ON	ON	OFF	ON
+2.5V_MEM	DDR4/L-RS +2.5V power rail	ON	ON	ON	OFF	ON
+1.8V_PRIM	System +1.8V power rail	ON	ON	OFF	ON*	ON
+1.8VS	System +1.8VS power rail	ON	OFF	OFF	OFF	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON	ON
+3.3V_ALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	OFF	ON*	ON
+3VS	System +3VS power rail	ON	OFF	OFF	OFF	ON
+3VGS	+3VS power rail for GPU	ON	OFF	OFF	OFF	ON
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF	OFF	ON
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	OFF	OFF	OFF	ON
+RTC_CELL	RTC power	ON	ON	ON	ON	ON
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF						

High Speed I/O (HSIO) Lane Multiplexing in KBL U PCH-LP



USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 port3 , IO/B
3	USB2.0 Port2
4	TypeC
5	Camera
6	Card reader , IO/B
7	BT
8	Touch screen
9	Finger printer
10	WWAN , IO/B

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1			USB3.0 port1
USB3.0-2			WWAN , IO/B
USB3.0-3			USB3.0 port2
USB3.0-4			TypeC
USB3.0-5	PCIE-1		GPU
USB3.0-6	PCIE-2		GPU
	PCIE-3		GPU
	PCIE-4		GPU
	PCIE-5		10/100 LAN
	PCIE-6		WLAN
	PCIE-7	SATA-0	SATA HDD
	PCIE-8	SATA-1	SATA ODD
	PCIE-9		NVME SSD
	PCIE-10		NVME SSD
	PCIE-11	SATA-1*	NVME SSD
	PCIE-12	SATA-2	NVME SSD

Board ID & Model ID table

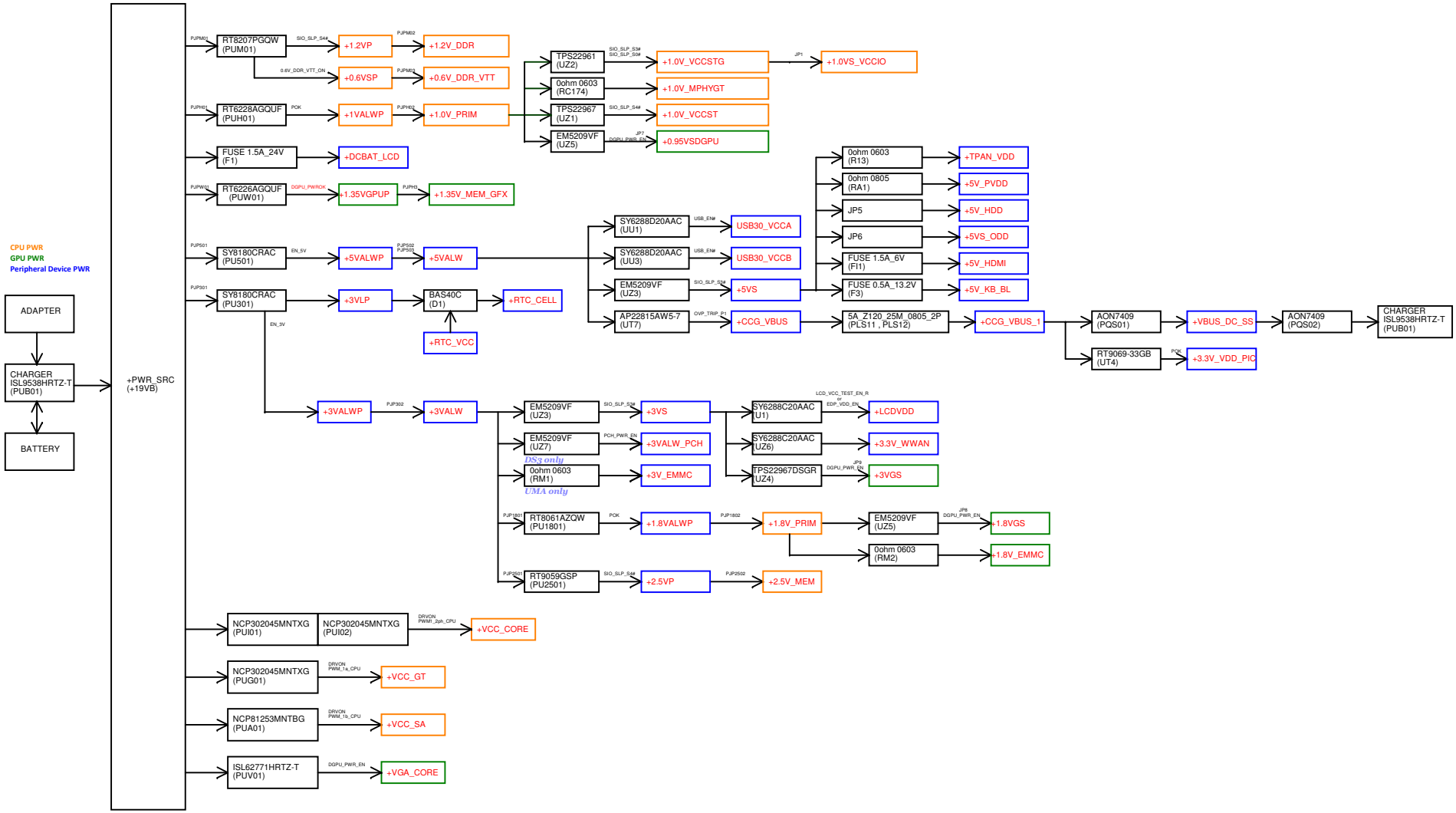
Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10.0	3.000	EVT
2	100	13.7	2.902	
3	100	17.8	2.801	DVT1
4	100	22.1	2.703	
5	100	27.0	2.598	DVT2
6	100	32.4	2.492	
7	100	37.4	2.402	
8	100	49.9	2.201	Pilot
9	100	57.6	2.094	
10	100	64.9	2.001	
11	100	73.2	1.905	
12	100	82.5	1.808	
13	100	93.1	1.709	
14	100	107.0	1.594	
15	100	120.0	1.500	
16	100	137.0	1.392	
17	100	154.0	1.299	
18	100	200.0	1.100	
19	100	232.0	0.994	

Compal Electronics, Inc.

Title: Index and Configuration

Size	Document Number	Rev
	LA-F115P	0.1

Date: Friday, July 28, 2017 Sheet 3 of 65



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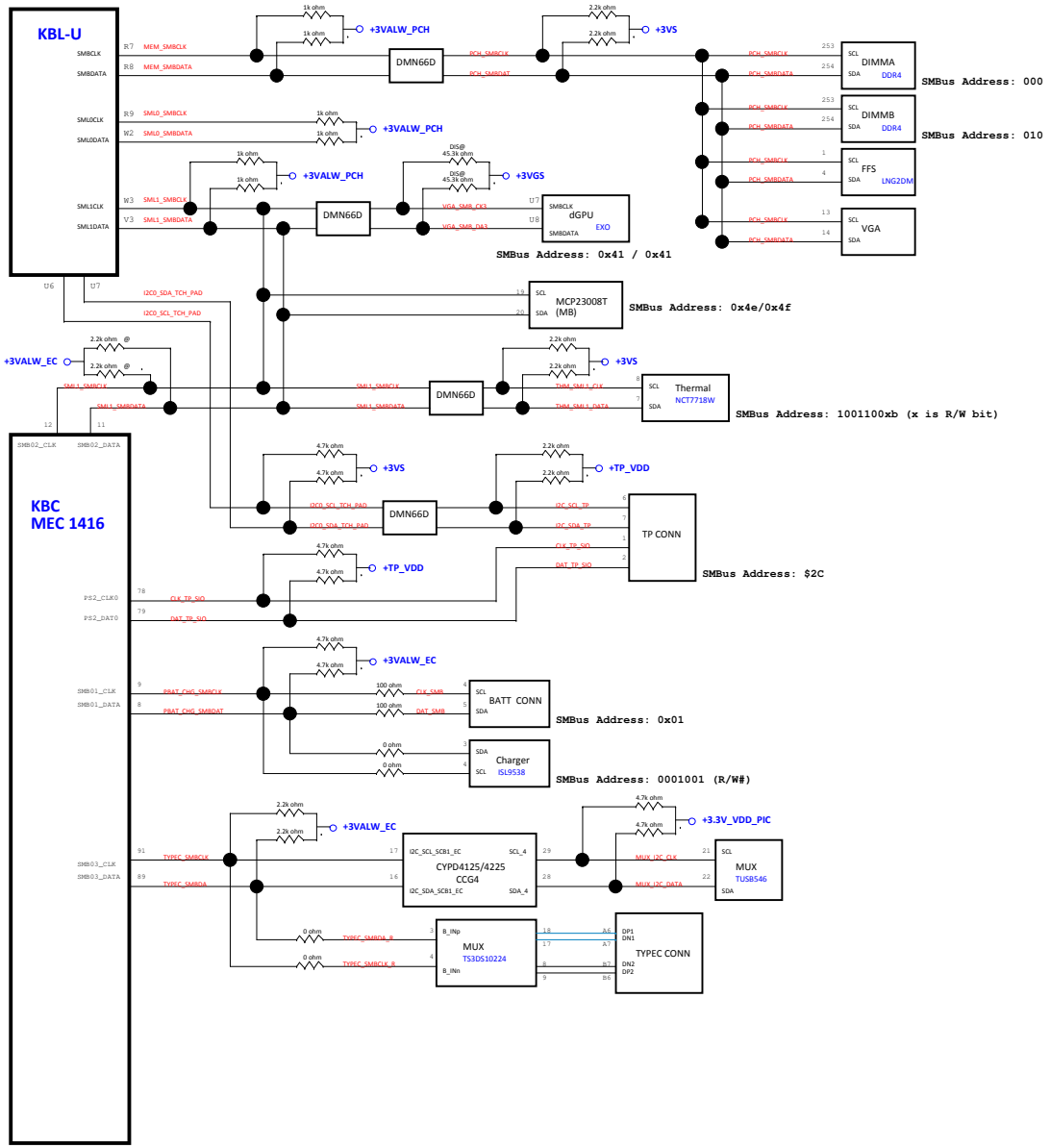
			Size: Document Number: LA-F115P Rev: 0.1
			Date: Friday, July 28, 2017 Sheet 4 of 65



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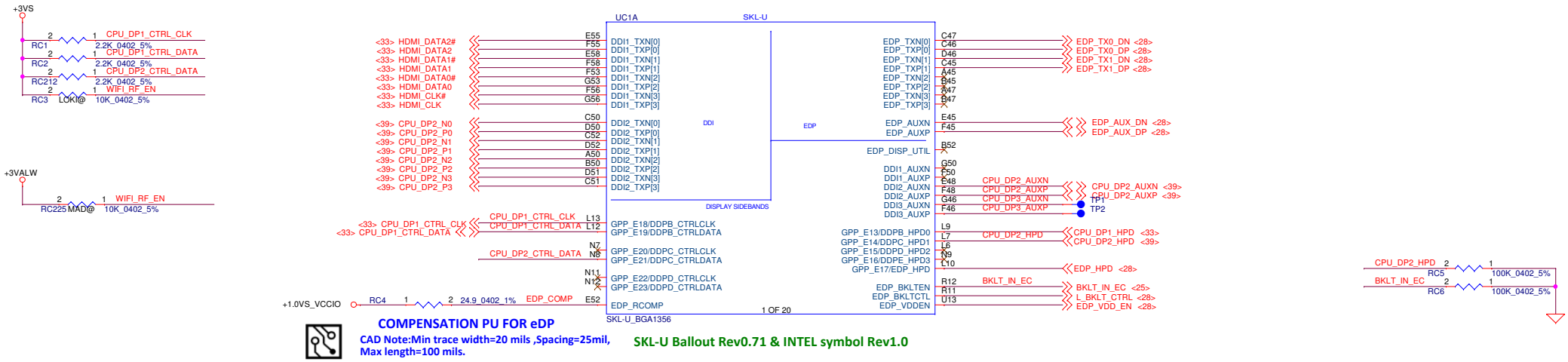
Issued Date	2016/12/01	Deciphered Date 2017/12/01	Title: SMbus Block Diagram
Size	Document Number: LA-F115P		Rev: 0.1
Date: Friday, July 28, 2017	Sheet 5 of 65		

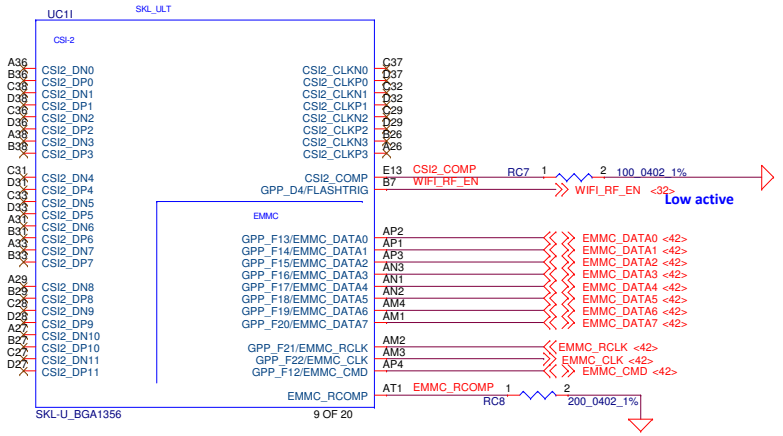
Main Func = CPU



COMPENSATION PU FOR eDP

CAD Note:Min trace width=20 mils ,Spacing=25mil, Max length=100 mils.

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0

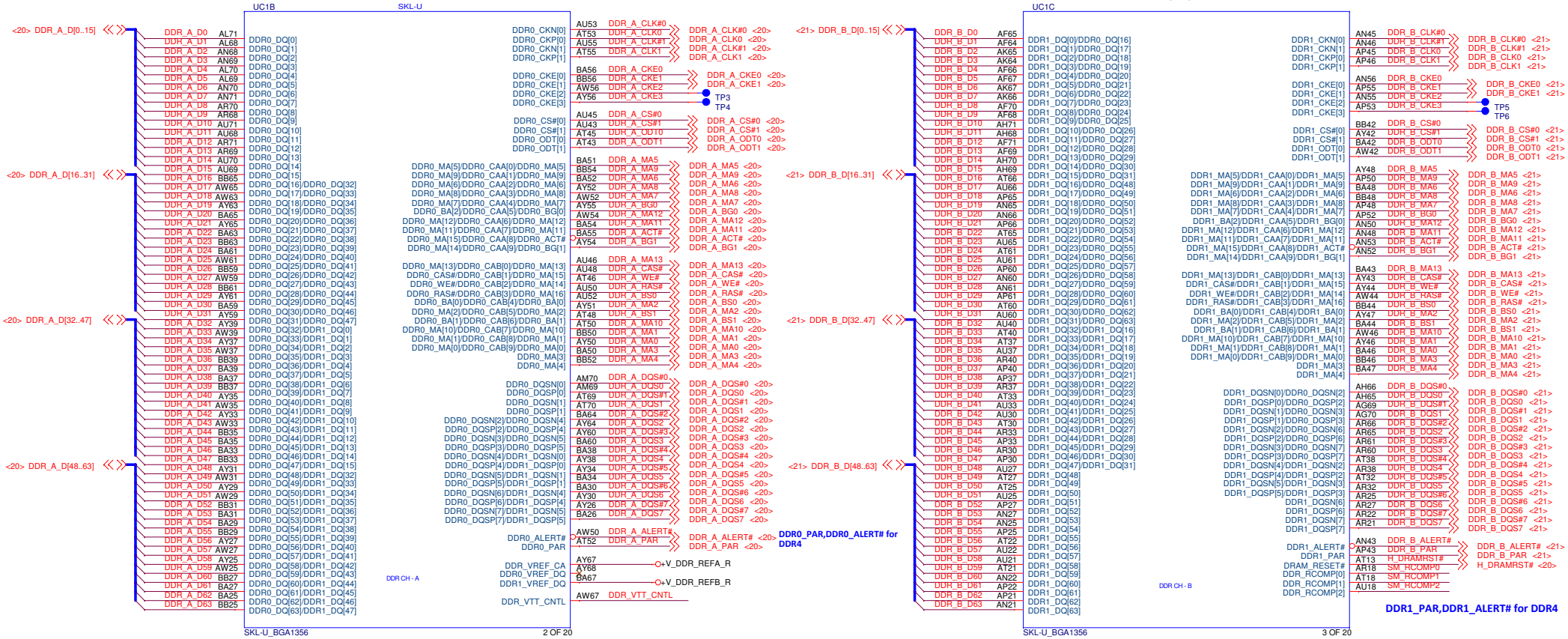


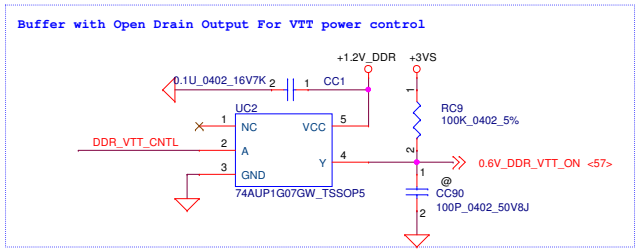
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

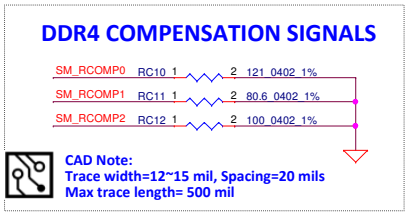
Compal Electronics, Inc.			
Title	MCP(1/14)DDI,EDP,CSI2,EMMC		
Size	Document Number LA-F115P		Rev 0.1
Date: Friday, July 28, 2017	Sheet 6 of 65		

Main Func = CPU

DDR4 Interleaved Memory







Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: MCP(2/14)DDR4			
Size	Document Number: LA-F115P		Rev: 0.1
Date: Friday, July 28, 2017		Sheet 7 of 65	

Main Func = CPU

SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

UC1E — SKL-U

SPI - FLASH
SPI0_CLK
SPI0_MISO
SPI0_MOSI
SPI0_IO2
SPI0_IO3
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#

SPI - TOUCH
GPP_D1/SPI1_CLK
GPP_D2/SPI1_MISO
GPP_D3/SPI1_MOSI
GPP_D21/SPI1_IO2
GPP_D22/SPI1_IO3
GPP_D0/SPI1_CS#

C LINK
CL_CLK
CL_DATA
CL_RST#

GPP_A0/RCIN#
GPP_A6/SERIRQ

SMBUS, SMLINK
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SML0CLK
GPP_C4/SML0DATA
GPP_C5/SML0ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
GPP_B23/SML1ALERT#/PCHHOT#

LPC
GPP_A1/LAD0/ESPI_IO0
GPP_A2/LAD1/ESPI_IO1
GPP_A3/LAD2/ESPI_IO2
GPP_A4/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A14/SUS_STAT#/ESPI_RESET#
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A8/CLKRUN#

SKL-U_BGA1356 — 5 OF 20

PCH_SPI_CLK RC2032 EMI@ 1 0_0402_5% AV2
PCH_SPI_D1 AW3
PCH_SPI_D0 AV3
PCH_SPI_D2 AW2
PCH_SPI_D3 AU4
PCH_SPI_CS#0 AU3
AU2
AU1
PCH_SPI_CS#2

TPM_SPI_IRQ# M2
M3
J4
V1
V2
M1

FFS_INT1 — RC35 10K_0402_5% — HDD_EN_PCH — Low active
HDD_DET#
HDD_EN_PCH — RC209 10K_0402_5%

CL_CLK G3
CL_DATA G2
CL_RST# G1

ESPI_ALERT# AW13
AY11
+1.8V_PRIM — RC14 10K_0402_5%

MEM_SMBCLK R7
MEM_SMBDATA R8
SMB_ALERT# R10
SML0_SMBCLK R9
SML0_SMBDATA W2
GPP_C5 W1
SML1_SMBCLK W3
SML1_SMBDATA V3
GPP_B23 AM7

SML1_SMBCLK <25,30,34,45>
SML1_SMBDATA <25,30,34,45>

PCH_ESPI_IO0 AY13
PCH_ESPI_IO1 BA13
PCH_ESPI_IO2 BB13
PCH_ESPI_IO3 AY12
ESPI_CS# BA12
ESPI_RESET# BA11
PCH_ESPI_CLK AW9
AY9
AW11

RPC2 — 15_0804_8P4R_5%
ESPI_IO0 <25>
ESPI_IO1 <25>
ESPI_IO2 <25>
ESPI_IO3 <25>
ESPI_CS# <25>
ESPI_RESET# <25>
ESPI_CLK <25>
RC15 EMI@ 1 2 22_0402_5%
MAD@RF@ CC88 82P_0402_50V8J

+3VS
QC1A DMN66D0LDW-7_SOT363-6
MEM_SMBCLK — PCH_SMBCLK <20,21,31,34>
QC1B DMN66D0LDW-7_SOT363-6
MEM_SMBDATA — PCH_SMBDATA <20,21,31,34>

SMB -> DDR4, FFS
SML1 -> EC, DGPU, THM

CLOSE TO UC1
@RF@ CC94 MEM_SMBCLK 33P_0402_50V8J
@RF@ CC95 SML0_SMBCLK 33P_0402_50V8J
@RF@ CC96 SML1_SMBCLK 33P_0402_50V8J

+3VS
PCH_SMBDATA — 2.2K_0402_5% — RC27
PCH_SMBCLK — 2.2K_0402_5% — RC28

+3VALW_PCH
MEM_SMBCLK — RC29 1K_0402_5%
MEM_SMBDATA — RC30 1K_0402_5%
SML1_SMBCLK — RC31 1K_0402_5%
SML1_SMBDATA — RC32 1K_0402_5%
SML0_SMBCLK — RC33 1K_0402_5%
SML0_SMBDATA — RC34 1K_0402_5%

+3VALW_PCH — +3.3V_SPI — RC17 @ 0_0603_5%

<14> XDP_SPI_SI — RC40 CMC@ 1K_0402_1% — PCH_SPI_D0
<14> XDP_SPI_IO2 — RC41 CMC@ 1K_0402_1% — PCH_SPI_D2
RC40/41 place to within 1100 mil of SPIO_MOSI/SPI0_IO2 pin for XDP

+3.3V_SPI — RC18 4.7K_0402_5% — PCH_SPI_CS#0

+3.3V_SPI — MOW 2015WW06
RC19 1K_0402_5% — PCH_SPI_D2
RC20 @ 1K_0402_5% — PCH_SPI_D3

+3.3V_SPI — CC3 0.1U_0402_25V6

UC3 — W25Q128FVSIQ_SO8
CS# VCC
WP# SCLK
HOLD# SI/SIO0
GND SO/SIO1

PCH_SPI_D2 — RC176 TPM@ 15_0402_5% — PCH_SPI_D2_R
PCH_SPI_D3 — RC177 TPM@ 15_0402_5% — PCH_SPI_D3_R
PCH_SPI_CS#0
PCH_SPI_CLK_R — RC178 TPM@ 15_0402_5% — PCH_SPI_CLK
PCH_SPI_D0_R — RC179 TPM@ 15_0402_5% — PCH_SPI_D0
PCH_SPI_D1_R — RC180 TPM@ 15_0402_5% — PCH_SPI_D1

RC178,RC179,RC180 place colse to UC1

128Mb Flash ROM

UC3 place colse to UX1

RC176 TPM@ 33_0402_5% SD028330A80
RC177 TPM@ 33_0402_5% SD028330A80
RC178 TPM@ 33_0402_5% SD028330A80
RC179 TPM@ 33_0402_5% SD028330A80
RC180 TPM@ 33_0402_5% SD028330A80

PCH_SPI_CLK_R — RC21 33_0402_5% @EMI@ — CC2 33P_0402_50V8J @EMI@

Int. PD. — +3VALW_PCH
SMB_ALERT# — RC37 @ 2.2K_0402_5%

TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Int. PD. — +3VALW_PCH
GPP_C5 — RC38 4.7K_0402_5%

EC interface	
HIGH	ESPI
LOW(DEFAULT)	LPC

+3VALW_PCH
Modify Value to 150k for WW52 MOW 2015/03/03 Jason
GPP_B23 — RC39 CMC@ 150K_0402_5%

EXI BOOT STALL BYPASS	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

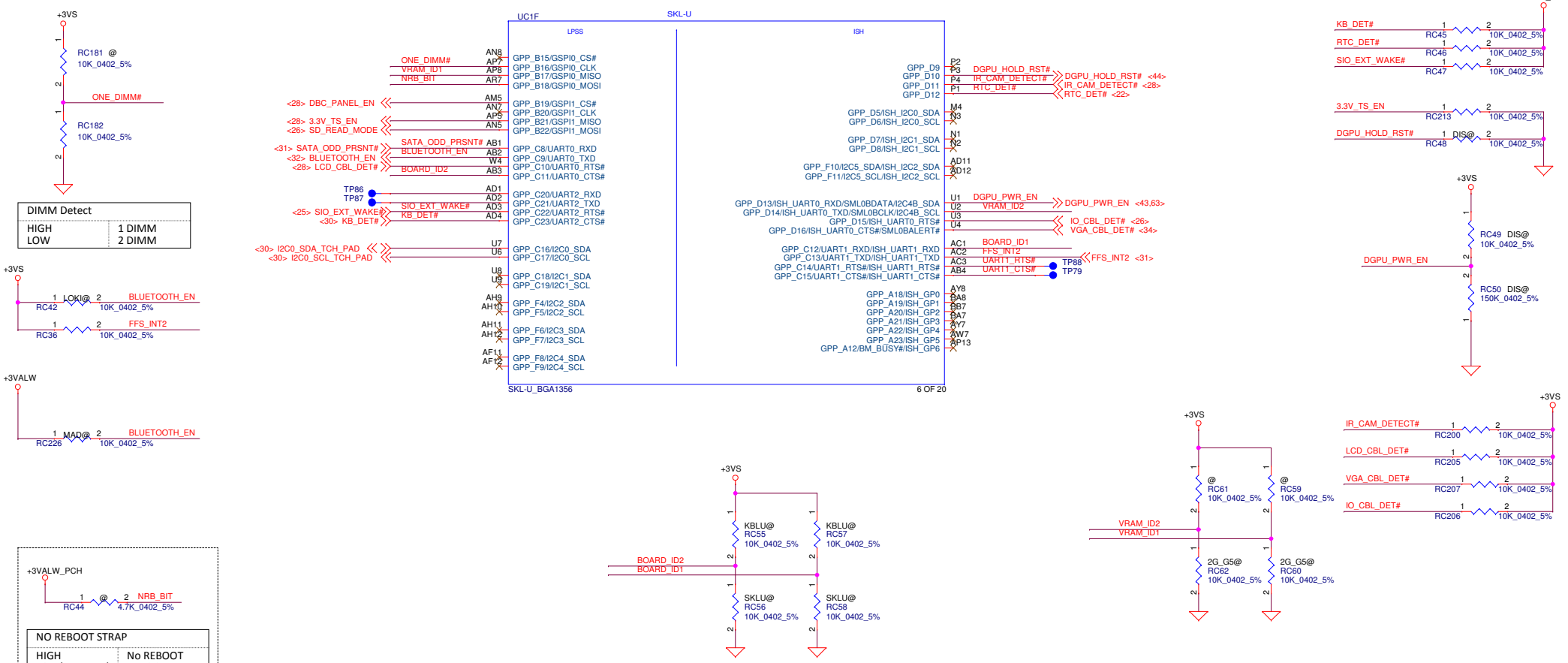
Compal Electronics, Inc.

Title: MCP(3/14)SPI,SMB,LPC

Size: | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 8 of 65

Main Func = CPU



CPU ID (PCBA VRAM Size Config.)	BOARD_ID2 (GPP_C11)	BOARD_ID1 (GPP_C12)
KBL-U	1	1
KBL-R	1	0
Reserved	0	1
SKL-U	0	0

RC55 KBLR@ 10K_0402_5% SD028100280

RC58 KBLR@ 10K_0402_5% SD028100280

VRAM ID (PCBA VRAM Size Config.)	VBIOS_ID2 (GPP_D14)	VBIOS_ID1 (GPP_B17)
2G GDDR5	0	0
4G GDDR5	0	1
Reserved	1	0
Reserved	1	1

RC62 4G_G5@ 10K_0402_5% SD028100280

RC59 4G_G5@ 10K_0402_5% SD028100280

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

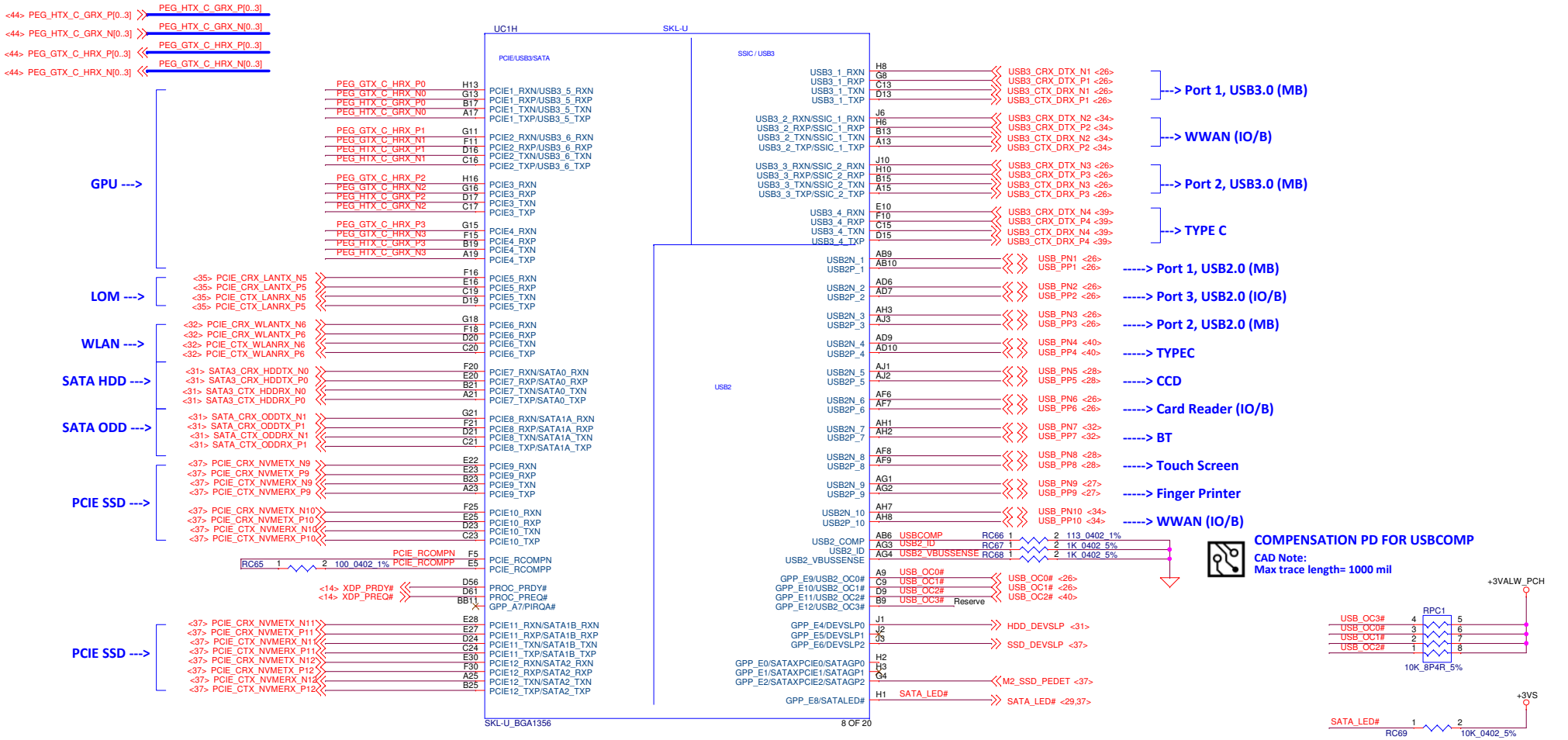
Compal Electronics, Inc.

Title: MCP(4/14)GSPI,I2C,UART,ISH

Size | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 9 of 65

Main Func = CPU

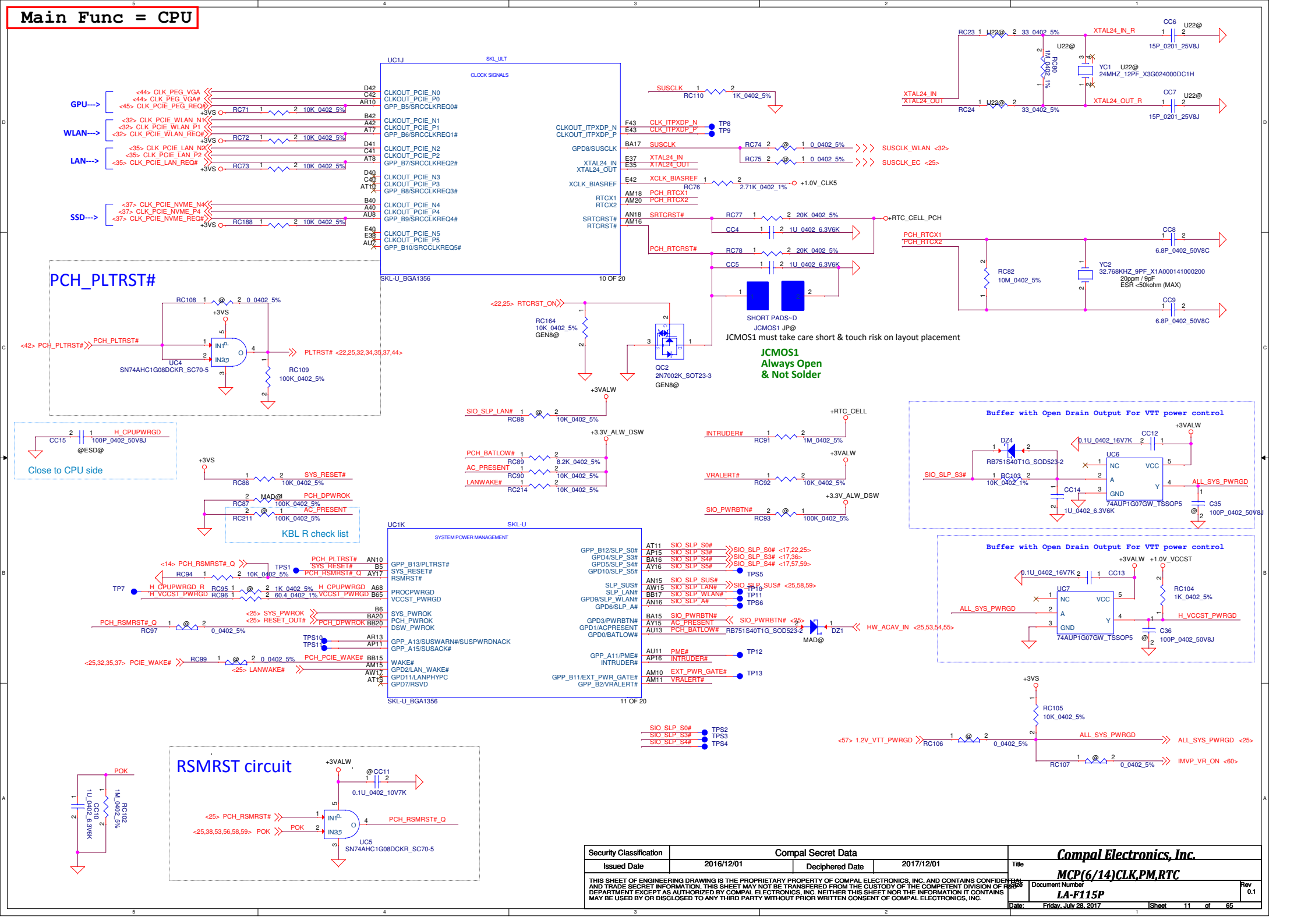


GPIO	Device Control
USB_OC0#	USB Port 1
USB_OC1#	WWAN
USB_OC2#	USB Port 4 (Type-C)
USB_OC3#	NA

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	MCP(5/14)PCIE,USB,SATA		
Size	Document Number	LA-F115P	Rev 0.1
Date: Friday, July 28, 2017	Sheet 10 of 65		

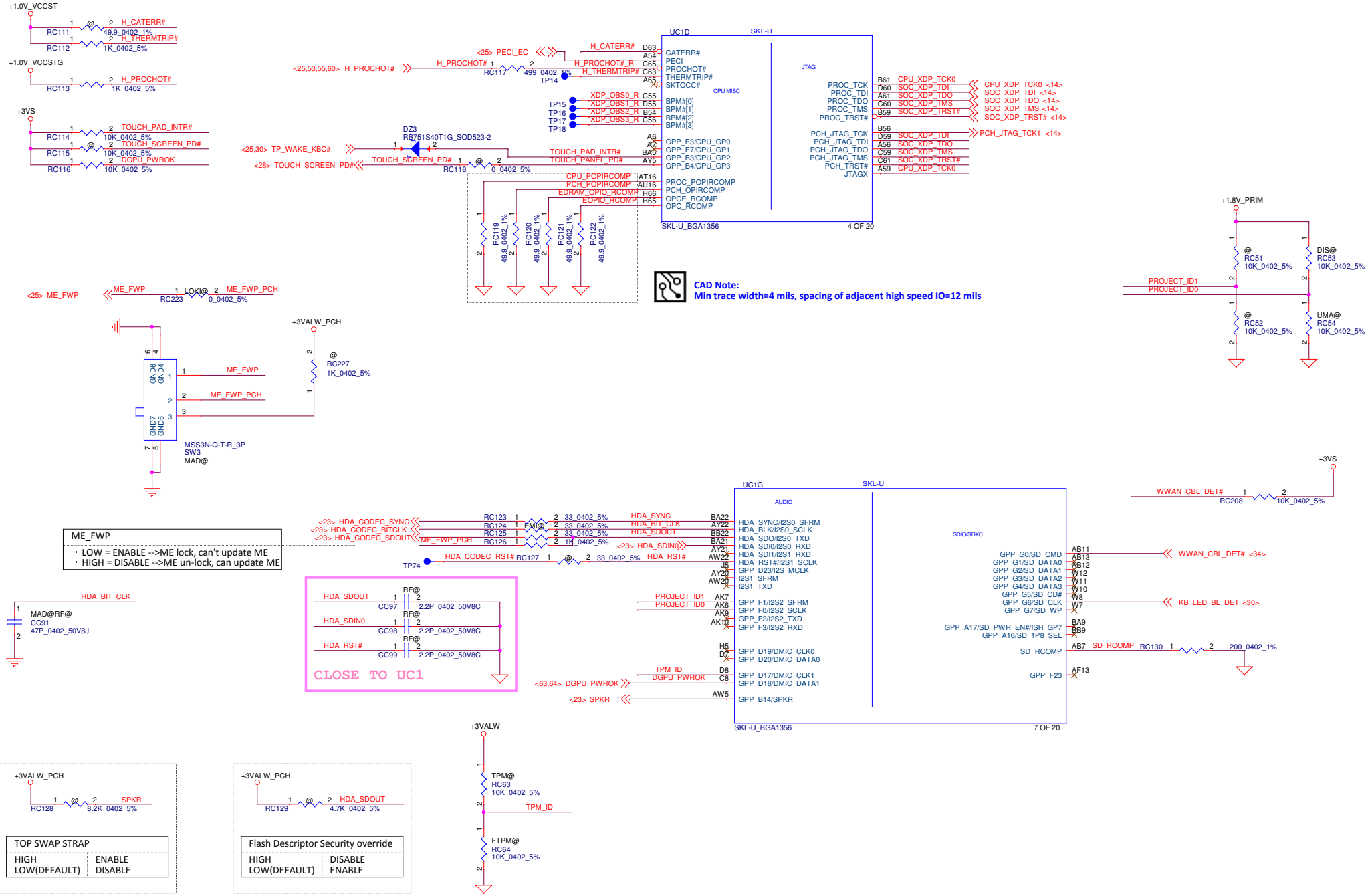
Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: MCP(6/14)CLK,PM,RTC			
Size	Document Number: LA-F115P		Rev: 0.1
Date: Friday, July 28, 2017	Sheet 11 of 65		

Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: MCP(7/14)MISC,JTAG,HDA,SDIO

Size: C | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 12 of 65

Main Func = CPU

RC131 1 @ 2 CFG0 10K_0402_1%

Stall reset sequence	
HIGH(DEFAULT)	No stall(Normal Operation)
LOW	stall

RC136 1 @ 2 CFG4 10K_0402_1%

eDP enable	
HIGH	Disabled
LOW(DEFAULT)	Enabled

RC132 1 @ 2 CFG1 10K_0402_1%
RC133 1 @ 2 CFG3 10K_0402_1%
RC134 2 1 CFG_RCOMP 49.9_0402_1%

UC1S SKL-U
RESERVED SIGNALS-1

<14> CFG0	CFG0 E68	CFG[0]	RSVD_TP_BB68 BB68 → TP21
<14> CFG1	CFG1 B67	CFG[1]	RSVD_TP_BB69 BB69 → TP22
<14> CFG2	D65	CFG[2]	
<14> CFG3	CFG3 D67	CFG[3]	RSVD_TP_AK13 AK13 → TP23
<14> CFG4	CFG4 E70	CFG[4]	RSVD_TP_AK12 AK12 → TP24
<14> CFG5	C68	CFG[5]	
<14> CFG6	D68	CFG[6]	RSVD_BB2 BB2
<14> CFG7	C67	CFG[7]	RSVD_BA3 BA3
<14> CFG8	F71	CFG[8]	
<14> CFG9	G69	CFG[9]	TP5 AU5 → TP25
<14> CFG10	F70	CFG[10]	TP6 AT5 → TP26
<14> CFG11	G68	CFG[11]	
<14> CFG12	H70	CFG[12]	RSVD_D5 D5
<14> CFG13	G71	CFG[13]	RSVD_D4 D4
<14> CFG14	H69	CFG[14]	RSVD_B2 B2
<14> CFG15	G70	CFG[15]	RSVD_C2 C2
<14> CFG16	E63	CFG[16]	RSVD_B3 B3
<14> CFG17	F63	CFG[17]	RSVD_A3 A3
<14> CFG18	E66	CFG[18]	RSVD_AW1 AW1
<14> CFG19	F66	CFG[19]	
	CFG_RCOMP E60	CFG_RCOMP	RSVD_E1 E1
<14> XDP_ITP_PMODE	E8	ITP_PMODE	RSVD_E2 E2
	AY2	RSVD_AY2	RSVD_BA4 BA4
	AY1	RSVD_AY1	RSVD_BB4 BB4
	D1	RSVD_D1	RSVD_A4 A4
	D3	RSVD_D3	RSVD_C4 C4
	K46	RSVD_K46	TP4 BB5 → TP27
	K45	RSVD_K45	
	AL25	RSVD_AL25	RSVD_A69 A69
	AL27	RSVD_AL27	RSVD_B69 B69
	C71	RSVD_C71	RSVD_AY3 AY3 1 @ 2 RC201 0_0402_5%
	B70	RSVD_B70	
	F60	RSVD_F60	RSVD_D71 D71
	A52	RSVD_A52	RSVD_C70 C70
			RSVD_C54 C54
			RSVD_D54 D54
TP19 TP20	BA70 BA68	RSVD_TP_BA70 RSVD_TP_BA68	TP1 AY4 → TP28
			TP2 BB3 → TP29
	J71	RSVD_J71	VSS_AY71 AY71 1 @ 2 RC202 0_0402_5%
	J68	RSVD_J68	ZVM# AR56
	F65	VSS_F65	RSVD_TP_AW71 AW71 → TP30
	G65	VSS_G65	RSVD_TP_AW70 AW70 → TP31
	F61	RSVD_F61	MSM# AP56
	E61	RSVD_E61	PROC_SELECT# C64 1 @ 2 RC138 100K_0402_5% +1.0V_VCCST

SKL-U_BGA1356 19 OF 20

From WW48 MOW

Stuff 100k(RC138) for Cannonlake

Un-stuff 100k(RC138) for Skylake

UC1T SKL-U
SPARE

AW69	RSVD_AW69	RSVD_F6 F6
AW68	RSVD_AW68	RSVD_E3 E3 KBLR_XTAL_IN
AU56	RSVD_AU56	RSVD_C11 C11
AW48	RSVD_AW48	RSVD_B11 B11
KBLR_XTAL_OUT C7	RSVD_C7	RSVD_A11 A11
RC137 1 @ 2 0_0402_5% U12	RSVD_U12	RSVD_D12 D12
U11	RSVD_U11	RSVD_C12 C12
H11	RSVD_H11	RSVD_F52 F52

+1.8V_PRIM

SKL-U_BGA1356 20 OF 20

RC25 1 U42@ 2 33_0402_5% KBLR_XTAL_IN_R 1 CC17 U42@ 2 12P_0201_25V8J

RC22 1M_0402_1% U42@

YC3 U42@ 24MHZ_12PF_X3G024000DC1H

KBLR_XTAL_IN
KBLR_XTAL_OUT
RC26 1 U42@ 2 33_0402_5% KBLR_XTAL_OUT_R 1 CC18 U42@ 2 12P_0201_25V8J

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

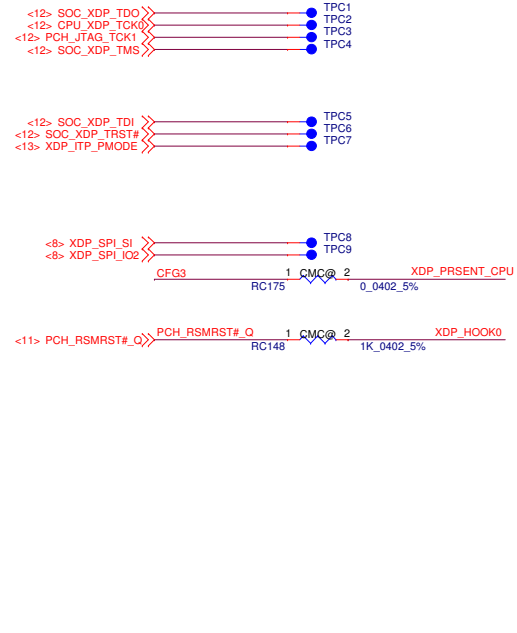
Title: MCP(8/14)CFG,RSVD

Size: C | Document Number: LA-F115P | Rev: 0.1

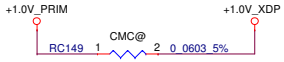
Date: Friday, July 28, 2017 | Sheet 13 of 65

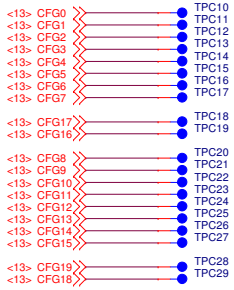
Main Func = CPU

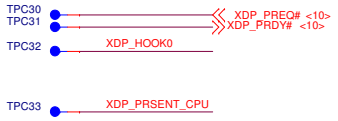
Connector Less Routing Topology



PRIMARY CMC CONN







Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: MCP(9/14)XDP			
Size	Document Number: LA-F115P		Rev: 0.1
Date: Friday, July 28, 2017		Sheet 14 of 65	

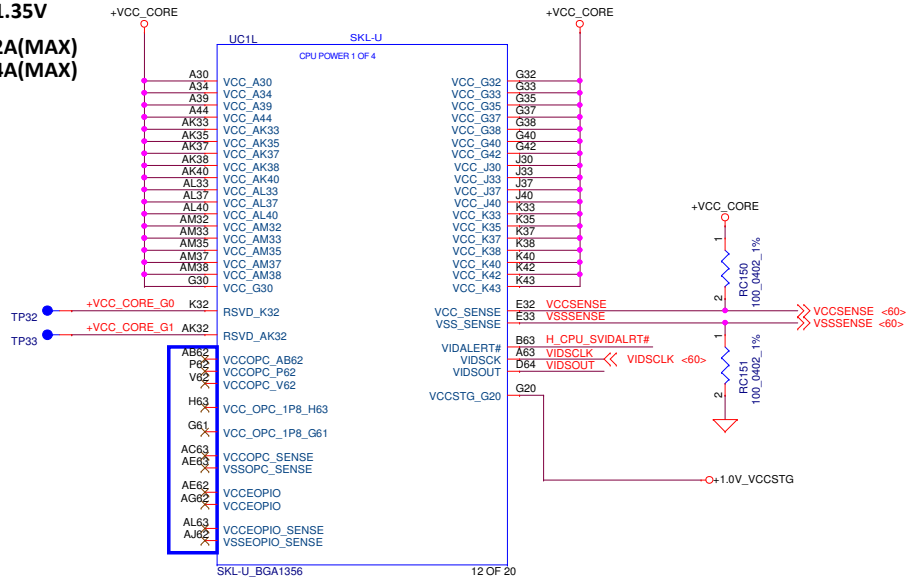
Main Func = CPU

PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

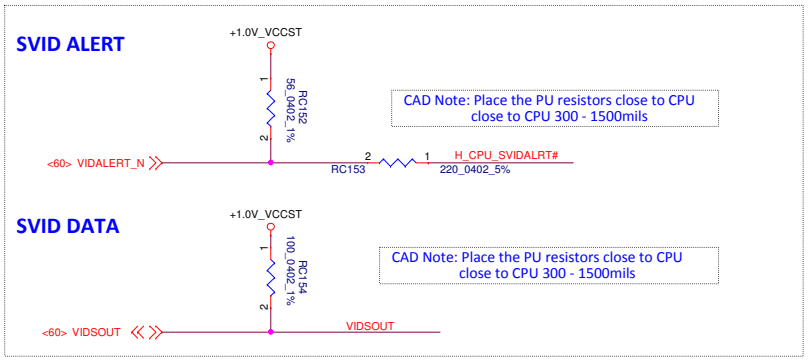
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

+VCC_CORE: 0.3~1.35V

+VCC_CORE(U22): 32A(MAX)
+VCC_CORE(U42): 64A(MAX)



VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: MCP(10/14)PWR-VCC CORE

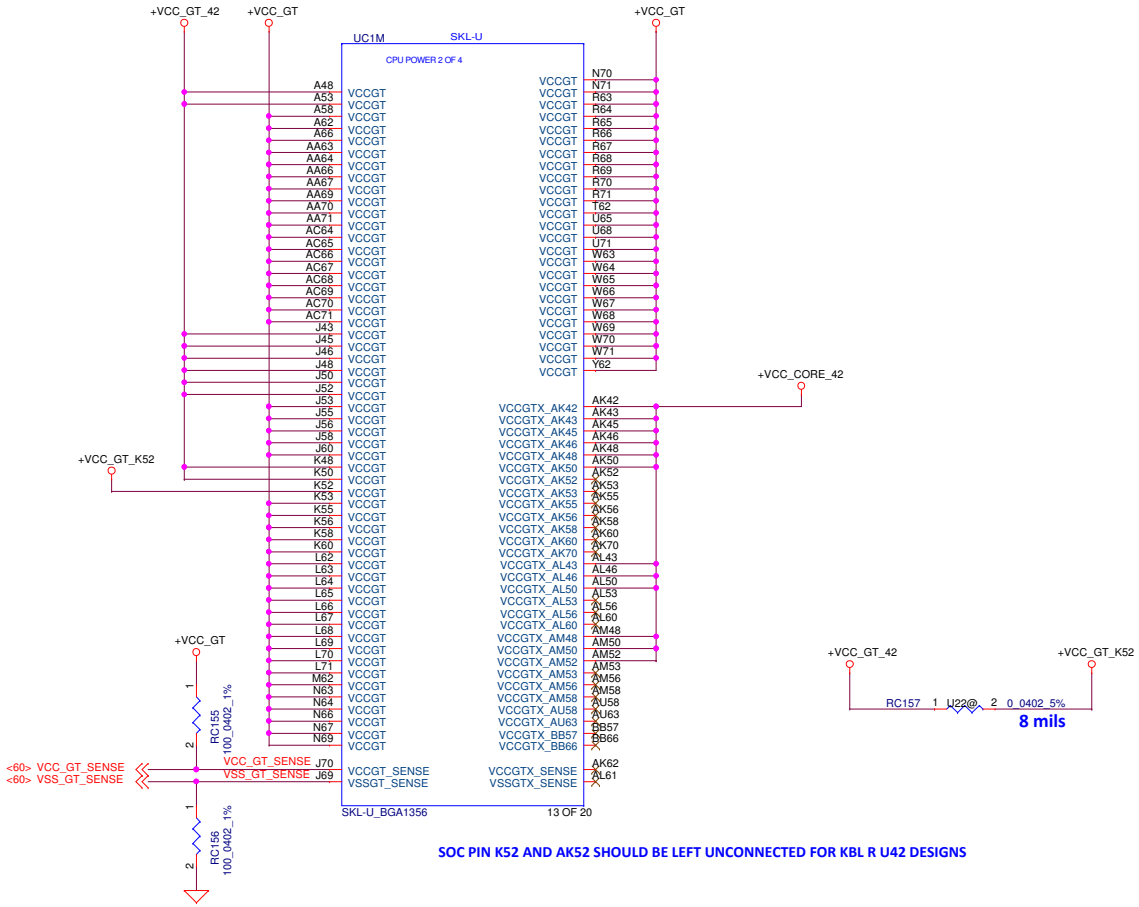
Size | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 15 of 65

Main Func = CPU

+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V

+VCC_GT(U22): 31A(MAX)
+VCC_GT(U42): 28A(MAX)



SOC PIN K52 AND AK52 SHOULD BE LEFT UNCONNECTED FOR KBL R U42 DESIGNS

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

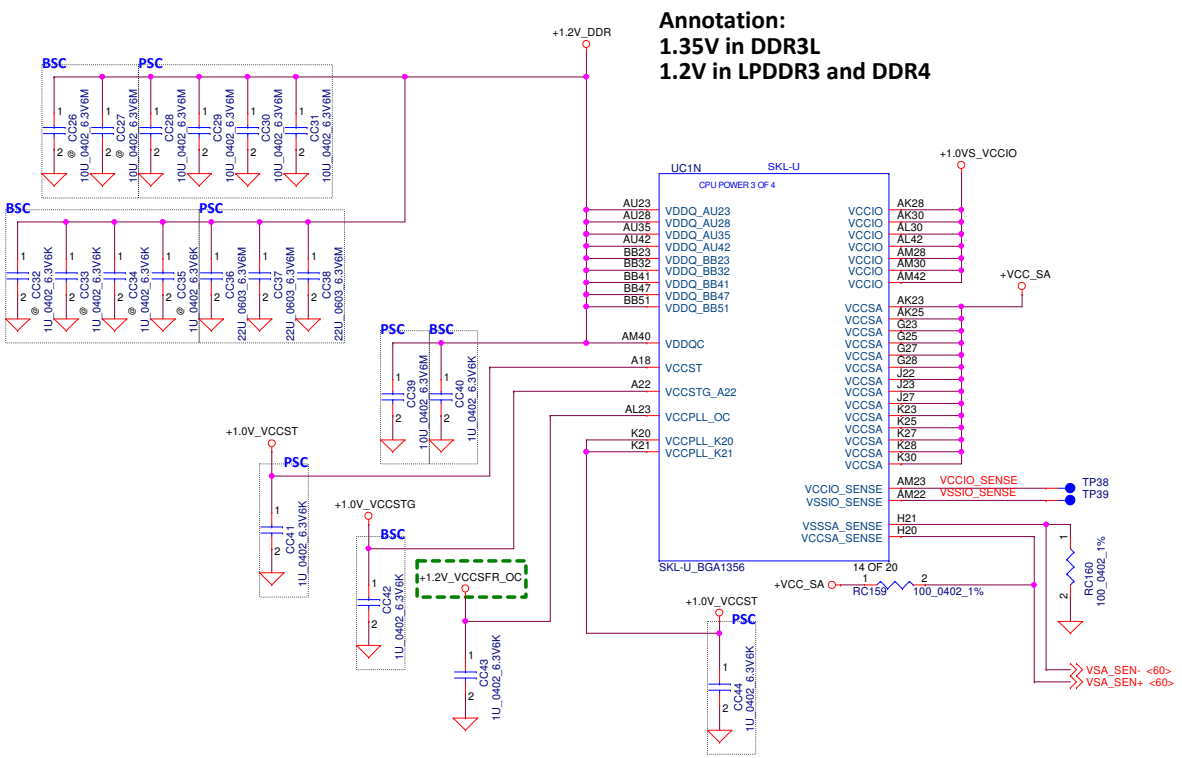
Title: MCP(11/14)PWR-VCCGT

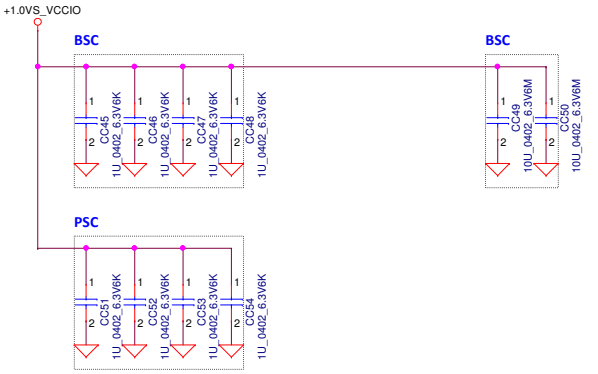
Size: C | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 16 of 65

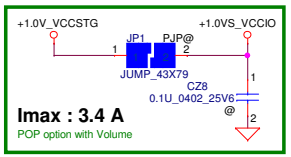
Main Func = CPU

Annotation:
1.35V in DDR3L
1.2V in LPDDR3 and DDR4





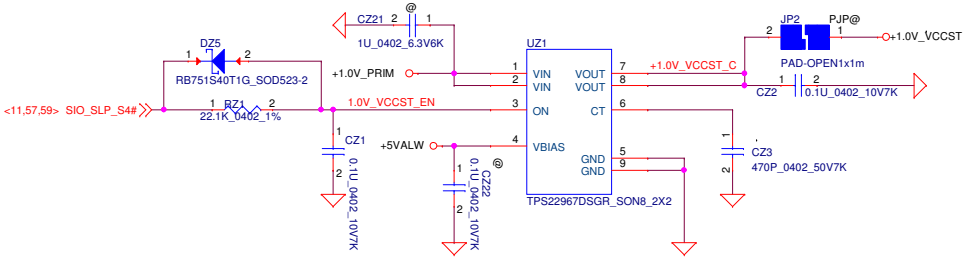
JP1
Always Short



+1.0V_VCCST source

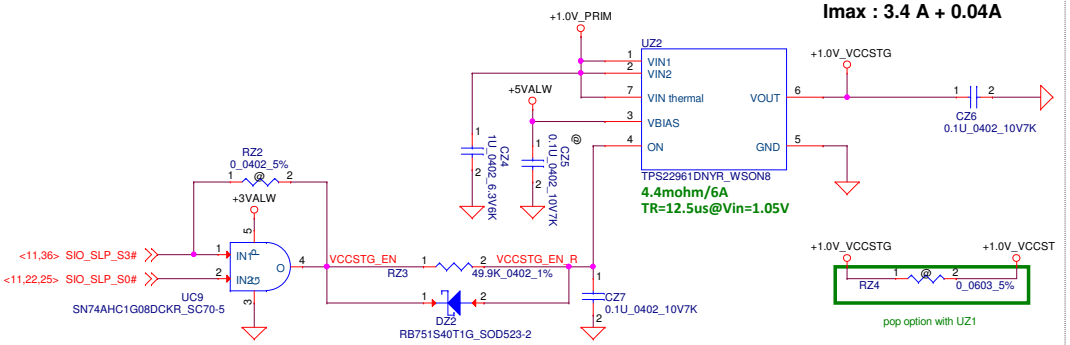
Imax : 0.24 A

JP2
Always Short



+1.0V_VCCSTG source

Imax : 3.4 A + 0.04A



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	MCP(12/14)PWR-VCCIO,MEM		
Size	Document Number	LA-F115P	Rev 0.1
Date: Friday, July 28, 2017	Sheet 17 of 65		

Main Func = CPU

+1.0V_MPHYGT source

+1.0V_PRIM — RC174 1 @ 2 0_0603_5% — +1.0V_MPHYGT

Imax : 2.8 A

PCH PWR

UC1O — SKL-U — CPU POWER 4 OF 4

SKL-U_BGA1356 — 15 OF 20

close UC1.AL1 and <120mil
close UC1.K17 and <120mil
close UC1.AB19 and <400mil
close UC1.AF18 and <400mil
close UC1.AF20 and <400mil
close UC1.N18 and <120mil
close UC1.Y16 and <400mil
close UC1.AG15 and <120mil
close UC1.T16 and <400mil
close UC1.V19 and <120mil
close UC1.AA1 and <400mil
close UC1.AK19 and <120mil
close UC1.BB10 and <120mil
close UC1.A10 and <120mil
close UC1.AJ19 and <100mil
close UC1.K15, UC1.L15 and <100mil
close UC1.K15 and <120mil
close UC1.K19 and <100mil
close UC1.L19 and <100mil
close UC1.AK17 and <120mil
close UC1.V15 and <100mil
close UC1.N20 and <100mil

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

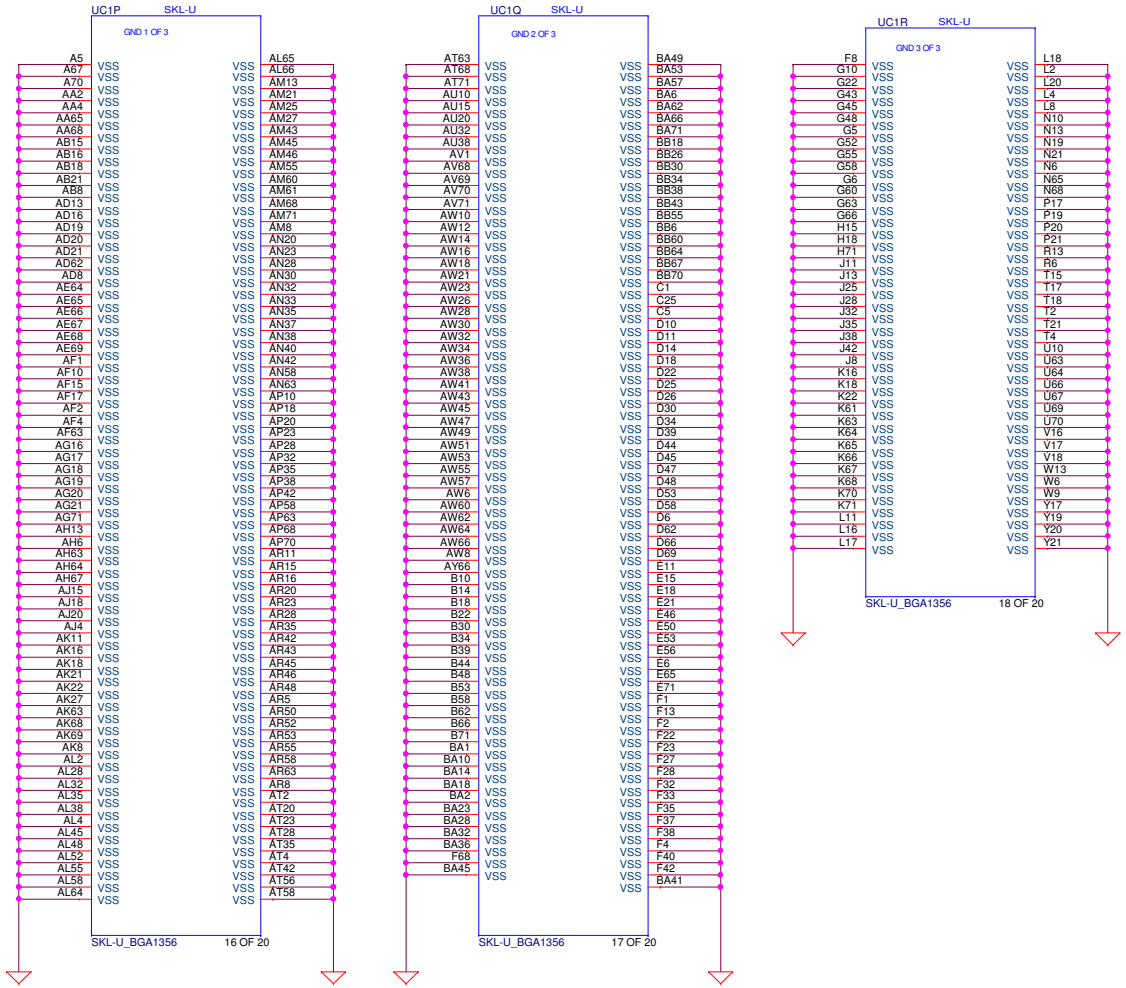
Compal Electronics, Inc.

Title: MCP(13/14)PCH PWR

Size: — Document Number: LA-F115P — Rev: 0.1

Date: Friday, July 28, 2017 — Sheet 18 of 65

Main Func = CPU



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: MCP(14/14)VSS

Size: C | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 19 of 65

Main Func = DDR

Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1

<7> DDR_A_D[0..63]
<7> DDR_A_MA[0..13]
<7> DDR_A_DQS#[0..7]
<7> DDR_A_DQS[0..7]

+2.5V_MEM
+0.6V_DDR_VTT
+3VS
+1.2V_DDR

CD1 10U_0603_6.3V6M-D
CD2 10U_0603_6.3V6M-D
CD3 1U_0402_6.3V6K-D
CD4 1U_0402_6.3V6K-D
CD5 1U_0402_6.3V6K-D
CD6 10U_0603_6.3V6M-D
CD7 10U_0603_6.3V6M-D
CD8 10U_0603_6.3V6M-D
CD9 0.1U_0402_16V7K-D
CD10 2.2U_0402_6.3V6M
CD11 1U_0402_6.3V6K-D
CD12 1U_0402_6.3V6K-D
CD13 1U_0402_6.3V6K-D
CD14 1U_0402_6.3V6K-D
CD15 1U_0402_6.3V6K-D
CD16 1U_0402_6.3V6K-D
CD17 1U_0402_6.3V6K-D
CD18 1U_0402_6.3V6K-D
CD19 10U_0603_6.3V6M-D
CD20 10U_0603_6.3V6M-D
CD21 10U_0603_6.3V6M-D
CD22 10U_0603_6.3V6M-D
CD23 10U_0603_6.3V6M-D
CD24 10U_0603_6.3V6M-D
CD25 10U_0603_6.3V6M-D
CD26 10U_0603_6.3V6M-D
CD27 330U_D2_2V_Y

RD1 0_0402_5%
RD2 0_0402_5%
RD3 0_0402_5%
RD4 0_0402_5%
RD5 0_0402_5%
RD6 0_0402_5%
RD7 470_0402_1%
RD8 0_0402_5%
RD9 2_0402_1%
RD10 1K_0402_1%~D
RD11 24.9_0402_1%
RD12 1K_0402_1%~D
RD23 240_0402_1%

DIMM_CHA_SA0
DIMM_CHA_SA1
DIMM_CHA_SA2

CD29 0.1U_0402_16V7K-D
CD30 0.022U_0402_25V7K

+V_DDR_REFA_R
+V_DDR_REFA
20mil

DDR4_DRAMRST#
H_DRAMRST# <7>

JDIMM1 CONN@

DDR_A_D1	VSS1	VSS2	DDR_A_D0
	DQ5	DQ4	
DDR_A_D5	VSS3	VSS4	DDR_A_D4
	DQ1	DQ0	
DDR_A_DQS#0	VSS5	VSS6	
DDR_A_DQS0	DQS0_c	DM0_n/DBI0_n	
	DQS0_t	VSS7	DDR_A_D6
DDR_A_D7	VSS8	DQ6	
	DQ7	VSS9	DDR_A_D2
DDR_A_D3	VSS10	DQ2	
	DQ3	VSS11	DDR_A_D12
DDR_A_D9	VSS12	DQ12	
	DQ13	VSS13	DDR_A_D13
DDR_A_D8	VSS14	DQ8	
	DQ9	VSS15	DDR_A_DQS#1
	VSS16	DQS1_c	DDR_A_DQS1
	DM1_n/DBI_n	DQS1_t	
DDR_A_D10	VSS17	VSS18	DDR_A_D15
	DQ15	DQ14	
DDR_A_D11	VSS19	VSS20	DDR_A_D14
	DQ10	DQ11	
DDR_A_D16	VSS21	VSS22	DDR_A_D21
	DQ21	DQ20	
DDR_A_D17	VSS23	VSS24	DDR_A_D20
	DQ17	DQ16	
	VSS25	VSS26	
DDR_A_DQS#2	DQS2_c	DM2_n/DBI2_n	
DDR_A_DQS2	DQS2_t	VSS27	DDR_A_D19
	VSS28	DQ22	
DDR_A_D22	DQ23	VSS29	DDR_A_D23
	VSS30	DQ18	
DDR_A_D18	DQ19	VSS31	DDR_A_D28
	VSS32	DQ28	
DDR_A_D24	DQ29	VSS33	DDR_A_D25
	VSS34	DQ24	
DDR_A_D29	DQ25	VSS35	DDR_A_DQS#3
	VSS36	DQS3_c	DDR_A_DQS3
	DM3_n/DBI3_n	DQS3_t	
	VSS37	VSS38	DDR_A_D31
DDR_A_D26	DQ30	DQ31	
	VSS39	VSS40	DDR_A_D27
DDR_A_D30	DQ26	DQ27	
	VSS41	VSS42	
	CB5/NC	CB4/NC	
	VSS43	VSS44	
	CB1/NC	CB0/NC	
	VSS45	VSS46	
	DQS8_c	DM8_n/DBI_n/NC	
	DQS8_t	VSS47	
	VSS48	CB6/NC	
	CB2/NC	VSS49	
	VSS50	CB7/NC	
	CB3/NC	VSS51	DDR4_DRAMRST#
	VSS52	RESET_n	DDR_A_CKE1
<7> DDR_A_CKE0	CKE0	CKE1	
DDR_A_CKE0	VDD1	VDD2	
<7> DDR_A_BG1	BG1	ACT_n	DDR_A_ALERT#
<7> DDR_A_BG0	BG0	ALERT_n	
	VDD3	VDD4	DDR_A_MA11
DDR_A_MA12	A12	A11	DDR_A_MA7
DDR_A_MA9	A9	A7	
	VDD5	VDD6	DDR_A_MA5
DDR_A_MA8	A8	A5	DDR_A_MA4
DDR_A_MA6	A6	A4	
	VDD7	VDD8	DDR_A_MA2
DDR_A_MA3	A3	A2	
DDR_A_MA1	A1	EVENT_n/NF	
	VDD9	VDD10	DDR_A_CLK1
DDR_A_CLK0	CK0_t	CK1_t/NF	DDR_A_CLK#1
<7> DDR_A_CLK0	CK0_c	CK1_c/NF	
<7> DDR_A_CLK#0	VDD11	VDD12	DDR_A_MA0
DDR_A_PAR	PARITY	A0	DDR_A_MA10
<7> DDR_A_PAR	BA1	A10/AP	
<7> DDR_A_BS1	VDD13	VDD14	DDR_A_BS0
DDR_A_CS#0	CS0_n	BA0	DDR_A_RAS#
<7> DDR_A_CS#0	WE_n/A14	RAS_n/A16	DDR_A_CAS#
<7> DDR_A_WE#	VDD15	VDD16	DDR_A_MA13
DDR_A_ODT0	ODT0	CAS_n/A15	
<7> DDR_A_ODT0	CS1_n	A13	
<7> DDR_A_CS#1	VDD17	VDD18	
DDR_A_ODT1	ODT1	C0/CS2_n/NC	TP40
<7> DDR_A_ODT1	VDD19	VREFCA	+V_DDR_REFA
	C1, CS3_n,NC	SA2	DIMM_CHA_SA2
TP41	VSS53	VSS54	
DDR_A_D36	DQ37	DQ36	DDR_A_D33
DDR_A_D37	VSS55	VSS56	DDR_A_D32
	DQ33	DQ32	
DDR_A_DQS#4	VSS57	VSS58	
DDR_A_DQS4	DQS4_c	DM4_n/DBI4_n	
	DQS4_t	VSS59	DDR_A_D38
DDR_A_D39	VSS60	DQ39	
DDR_A_D34	DQ38	VSS61	DDR_A_D35
	VSS62	DQ35	
DDR_A_D41	DQ34	VSS63	DDR_A_D45
	VSS64	DQ45	
DDR_A_D40	DQ44	VSS65	DDR_A_D44
	VSS66	DQ41	
	DQ40	VSS67	DDR_A_DQS#5
	VSS68	DQS5_c	DDR_A_DQS5
	DM5_n/DBI5_n	DQS5_t	
DDR_A_D43	VSS69	VSS70	DDR_A_D47
	DQ46	DQ47	
DDR_A_D42	VSS71	VSS72	DDR_A_D46
	DQ42	DQ43	
DDR_A_D48	VSS73	VSS74	DDR_A_D53
	DQ52	DQ53	
DDR_A_D52	VSS75	VSS76	DDR_A_D49
	DQ49	DQ48	
DDR_A_DQS#6	VSS77	VSS78	
DDR_A_DQS6	DQS6_c	DM6_n/DBI6_n	
	DQS6_t	VSS79	DDR_A_D54
DDR_A_D55	VSS80	DQ54	
	DQ55	VSS81	DDR_A_D51
DDR_A_D50	VSS82	DQ50	
	DQ51	VSS83	DDR_A_D59
DDR_A_D57	VSS84	DQ60	
	DQ61	VSS85	DDR_A_D58
DDR_A_D56	VSS86	DQ57	
	DQ56	VSS87	DDR_A_DQS#7
	VSS88	DQS7_c	DDR_A_DQS7
	DM7_n/DBI7_n	DQS7_t	
DDR_A_D60	VSS89	VSS90	DDR_A_D62
	DQ62	DQ63	
DDR_A_D61	VSS91	VSS92	DDR_A_D63
	DQ58	DQ59	
PCH_SMBCLK	VSS93	VSS94	PCH_SMBDATA
<8,21,31,34> PCH_SMBCLK	SCL	SDA	PCH_SMBDATA <8,21,31,34>
	VDDSPD	SA0	DIMM_CHA_SA0
+3VS	VPP1	VTT	+0.6V_DDR_VTT
+2.5V_MEM	VPP2	SA1	DIMM_CHA_SA1
	GND1	GND2	

LOTES_ADDR0206-P001A02~D
DEREN_40-42271-26001RHF
SP07001CY0L

All VREF traces should have 10 mil trace width

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: DDR4 DIMMA RVS

Size | Document Number: LA-F111P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 20 of 65

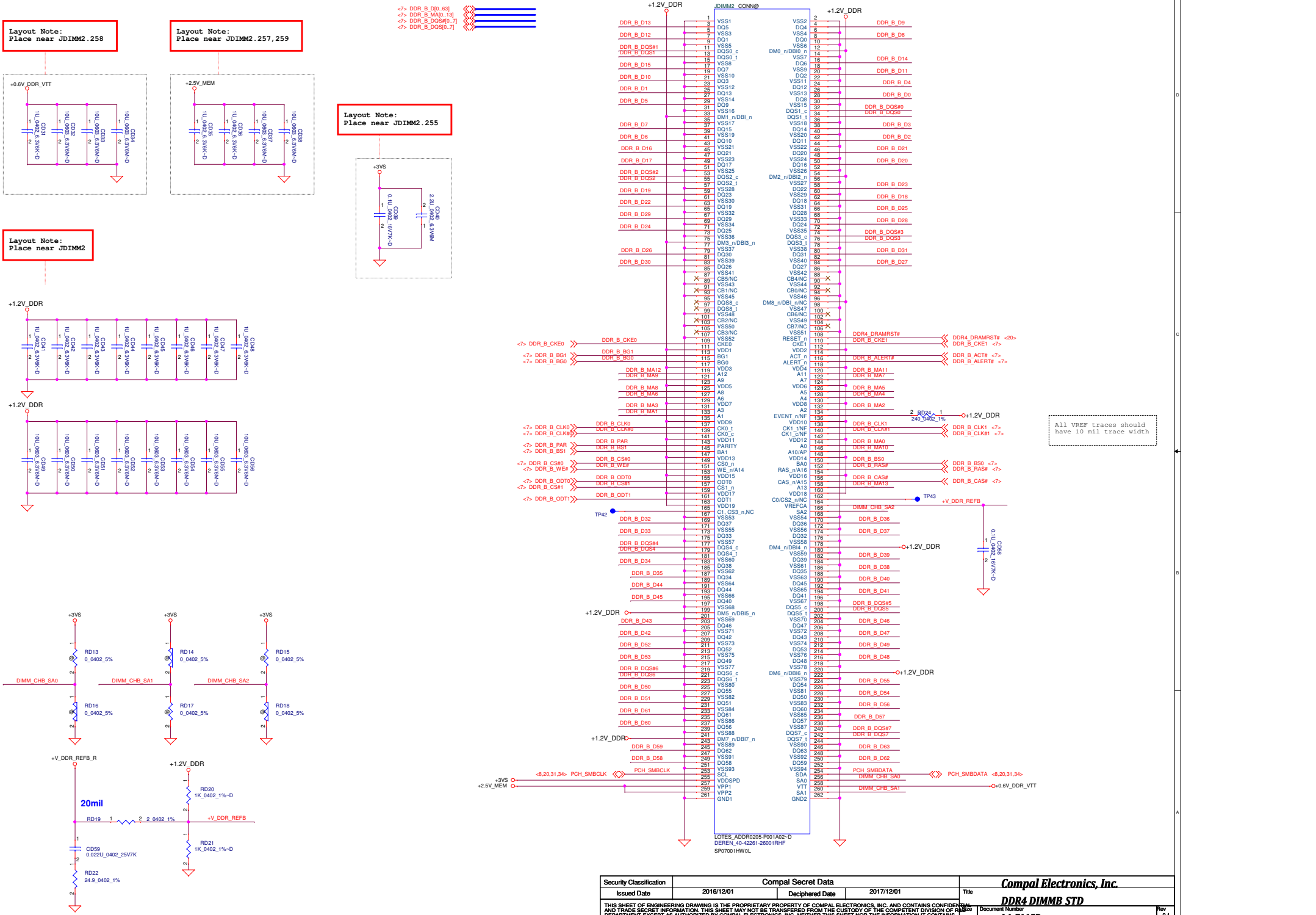
Main Func = DDR

Layout Note:
Place near JDIMM2.258

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.255

Layout Note:
Place near JDIMM2



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

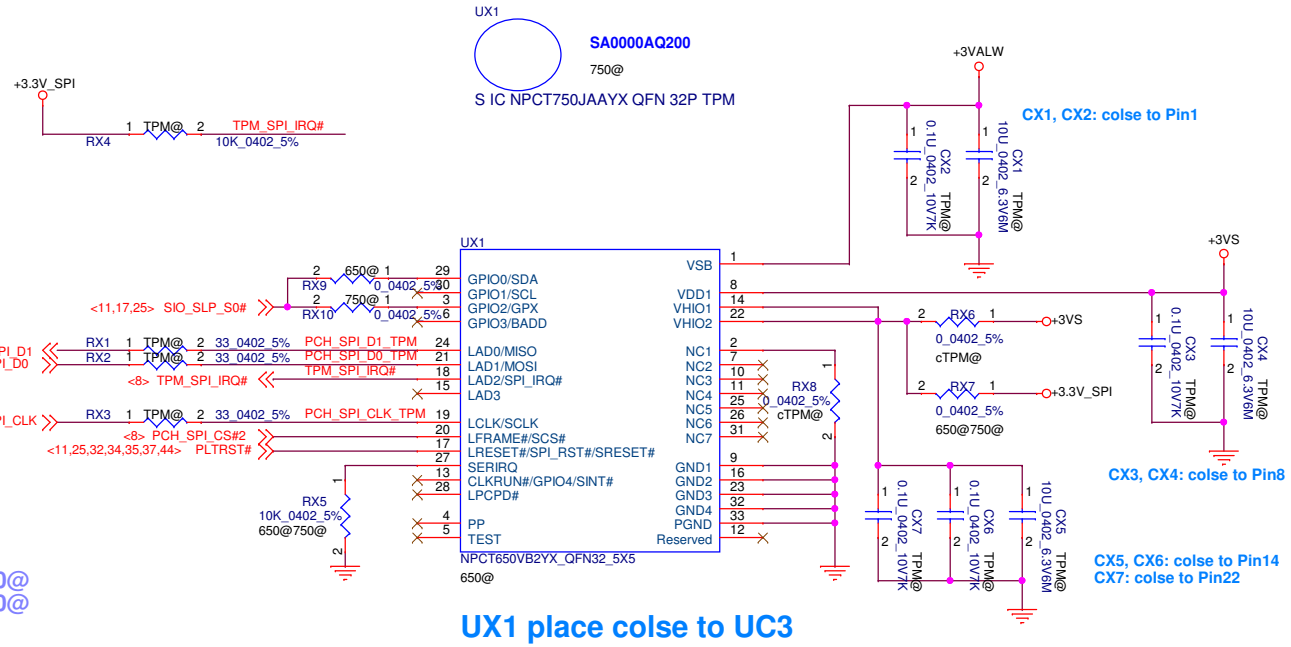
Compal Electronics, Inc.			
Title	DDR4 DIMMB STD		
Size	Document Number		Rev
	LA-F115P		0.1
Date:	Friday, July 28, 2017	Sheet	21 of 65

Main Func = TPM

Screw hole/FD

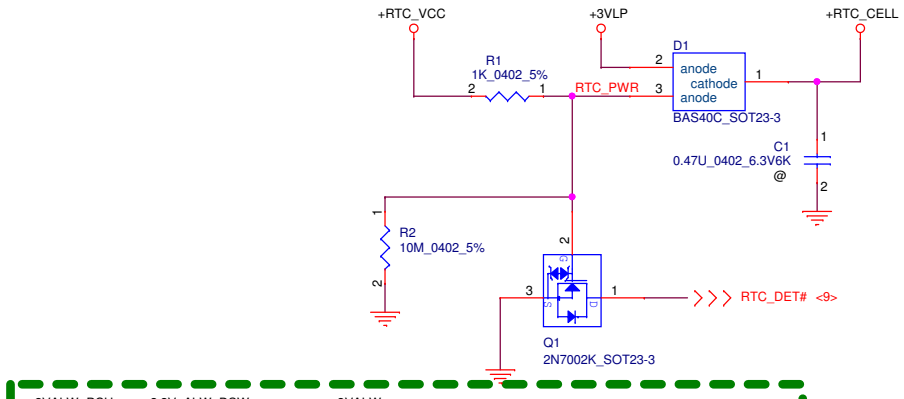
H1 HOLEA — H_3P0
H3 HOLEA — H_5P0
H4 HOLEA — H_3P0
H5 HOLEA — H_3P0-G
H6 HOLEA — H_3P0-G
H7 HOLEA — H_3P0
H8 HOLEA — H_3P3-G
H9 HOLEA — H_3P5
H10 HOLEA — H_3P5
H11 HOLEA — H_3P2
H12 HOLEA — H_3P2-G
H13 HOLEA — H_3P0X4P0
H14 HOLEA — H_5P6N
HCPU1 HOLEA — H_4P0X3P7
HCPU2 HOLEA — H_3P7
HCPU3 HOLEA — H_4P0
HCPU4 HOLEA — H_3P7X4P0
FD1
FD2
FD3
FD4

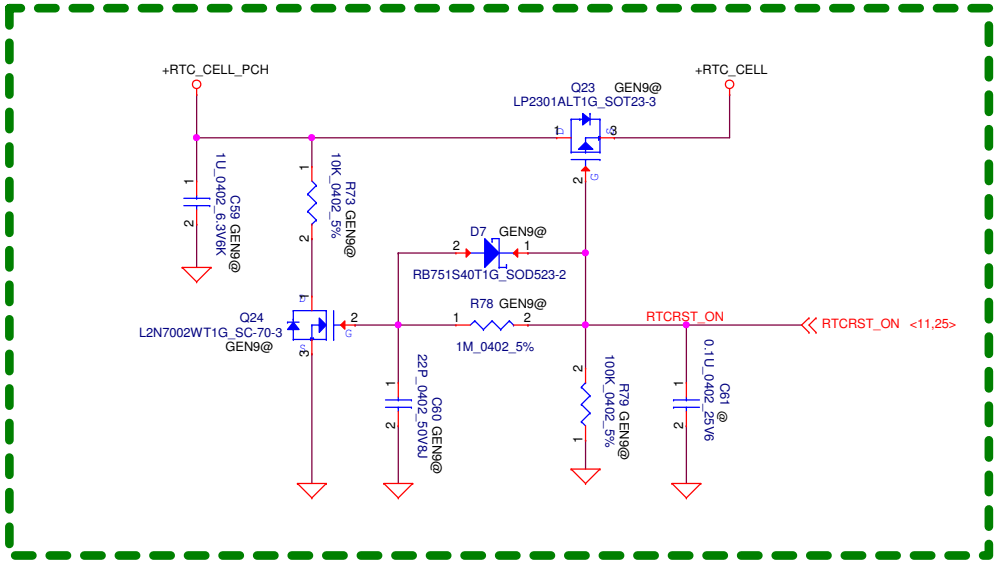
NPCT650:TPM@/650@/650@750@
NPCT750:TPM@/750@/650@750@
ChinaTPM:TPM@/cTPM@
SW TPM:fTPM@

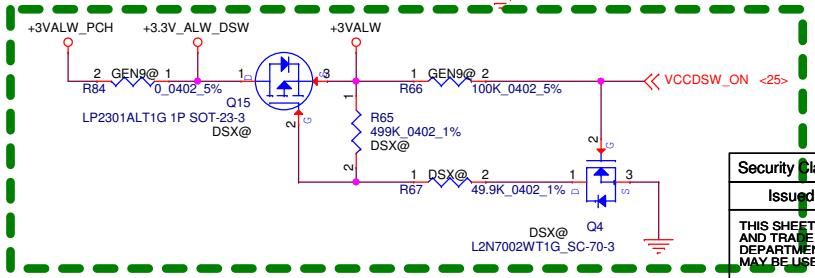


UX1 place colse to UC3

Main Func = RTC



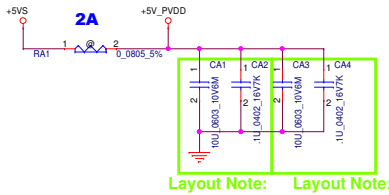


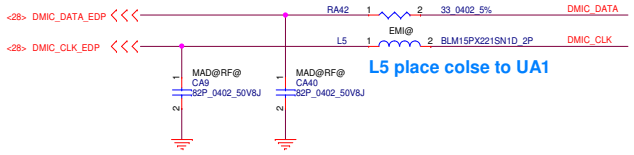


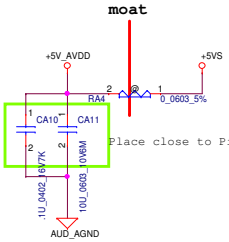
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

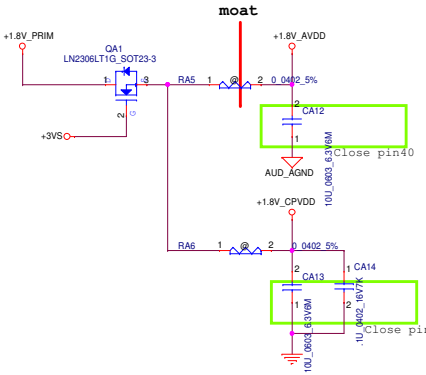
Compal Electronics, Inc.	
Title	TPM/RTC/Screw hole
Size	Document Number: LA-F115P
Rev	0.1
Date: Friday, July 28, 2017	Sheet 22 of 65

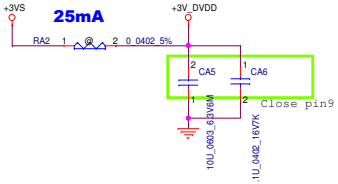
Main Func = Audio

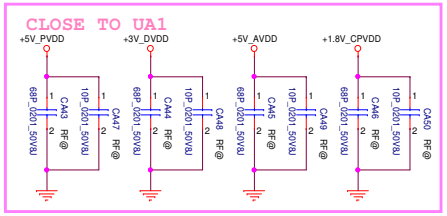


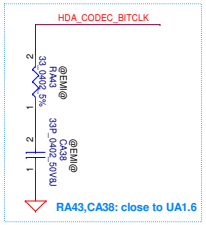


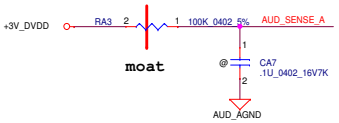


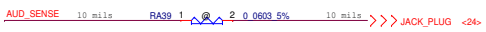


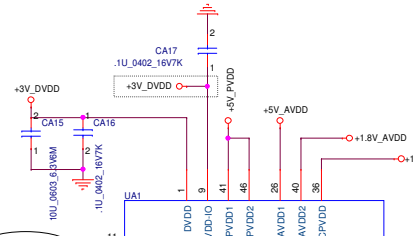


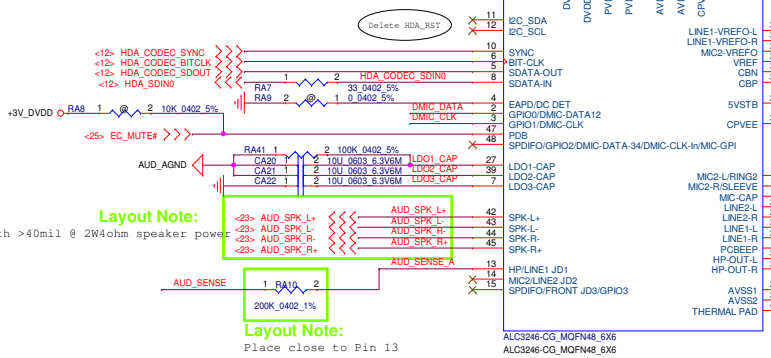


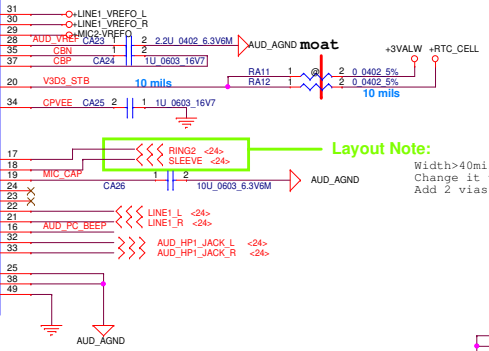


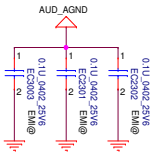


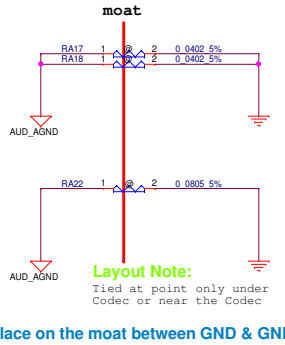


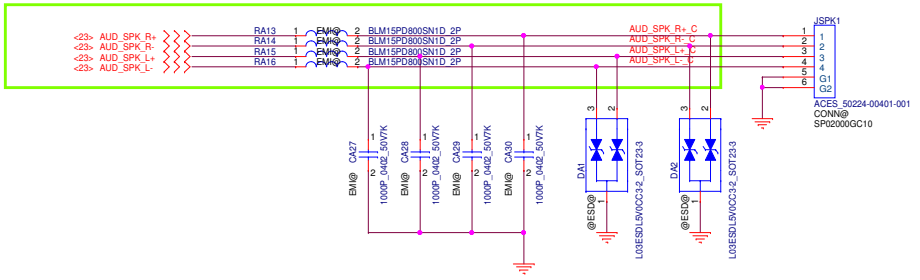




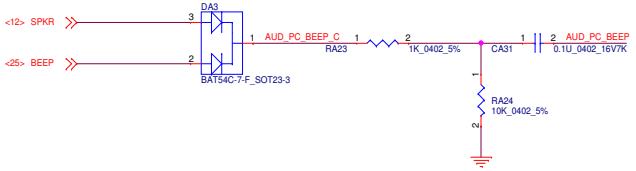








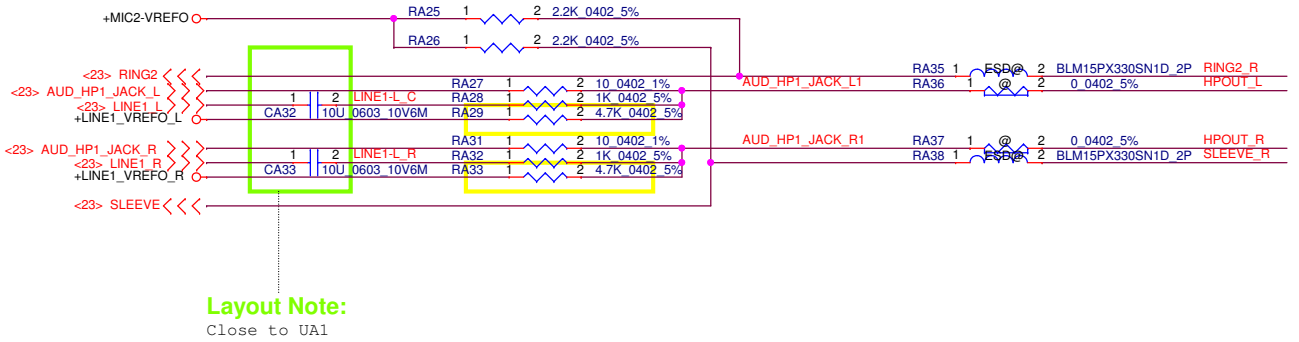
CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	Audio Codec ALC3246		
Size	Document Number	Rev	
	LA-F115P	0.1	
Date:	Friday, July 28, 2017	Sheet	23 of 65

Main Func = Audio Jack

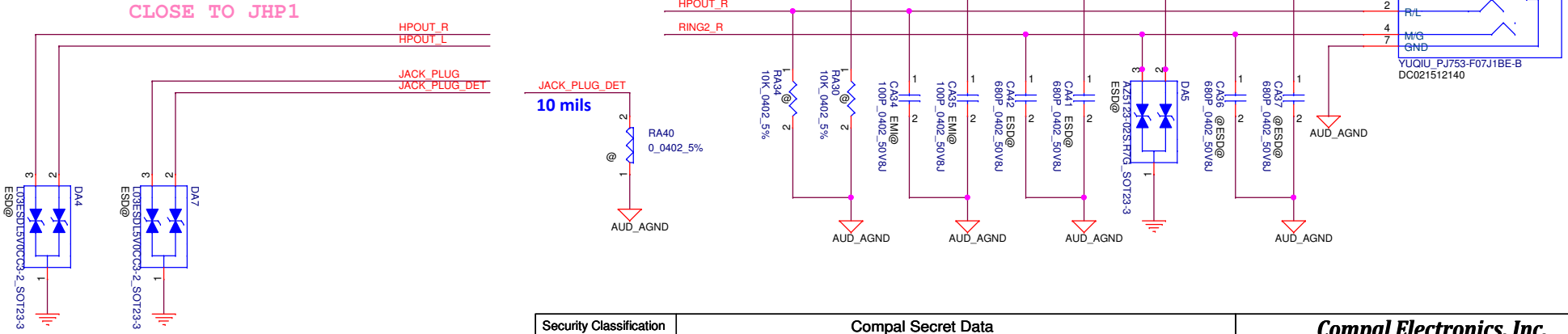


Universal Jack
(Global Headset Jack + mic phone in + line in support)

Layout Note:
Close to UA1

Main Func = Audio Jack

Universal Jack
(Global Headset Jack + mic phone in + line in support)



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: **Audio JACK**

Size | Document Number: **LA-F115P** | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 24 of 65

Main Func = EC

EC Chip CPN

MEC1416-NU-D0_VTQFP128_14X14

SA0000A8L00

SD034178280 for Loki-L

17.8K_0402_1%

SD034499280 for Loki

49.9K_0402_1%

For Board ID Select

EVT	10K	SD034200380
DVT1	17.8K	SD034232380
DVT2	27K	
Pilot	49.9K	SD034100380

Model ID

MODEL_ID

Board ID

BOARD_ID

MEC1416

+RTC_CELL

32 KHz Clock

Debug Connector

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

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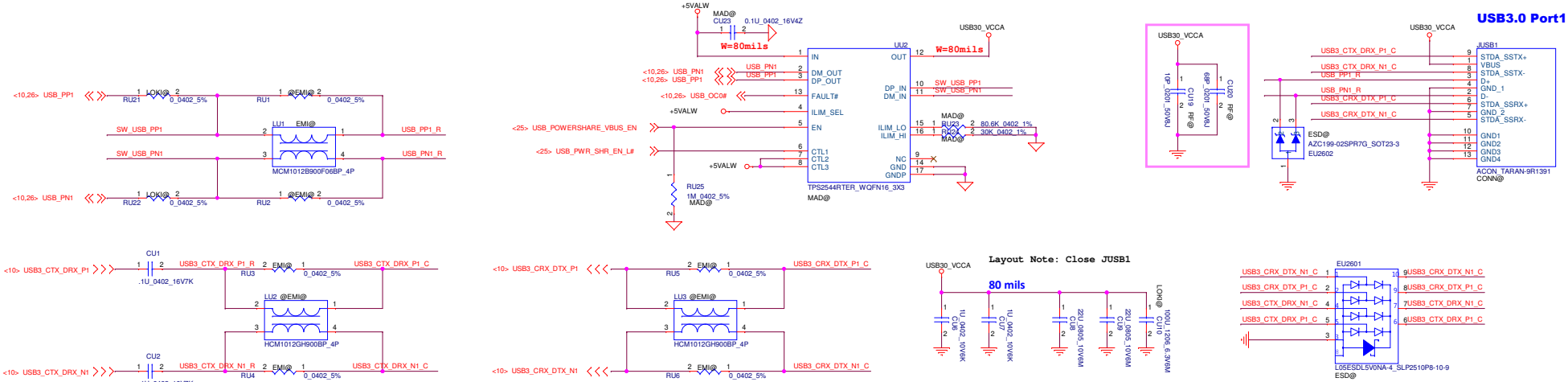
Compal Electronics, Inc.

Title: EC MEC1416

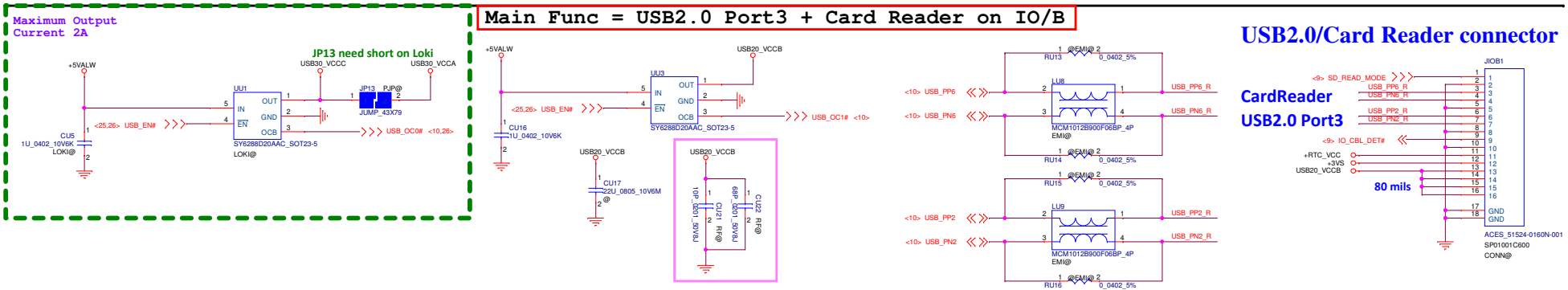
Size: | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 25 of 65

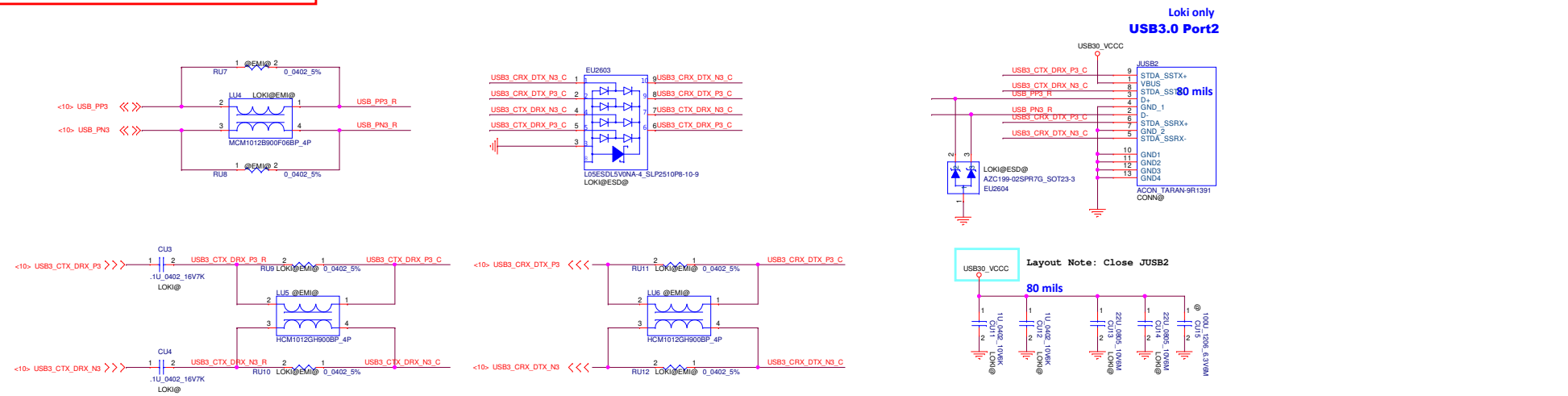
Main Func = USB3.0 Port1



Main Func = USB2.0 Port3 + Card Reader on IO/B



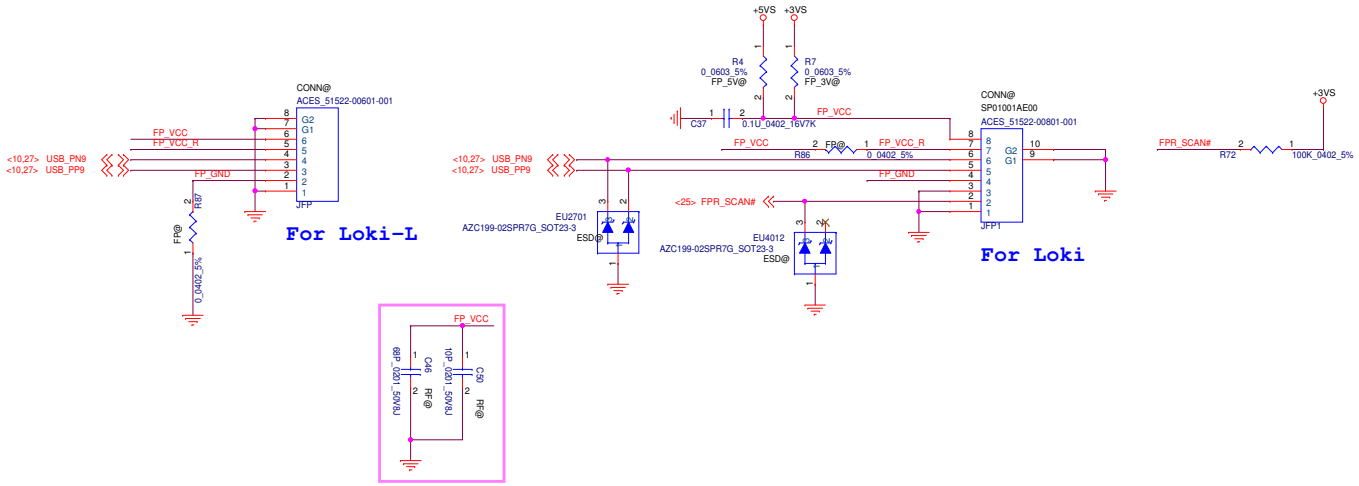
Main Func = USB3.0 Port2



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.	
Title	USB3.0 & I/O
Size	Document Number: LA-F115P
Rev	0.1
Date:	Friday, July 28, 2017
Sheet	26 of 65

Main Func = Finger Printer



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

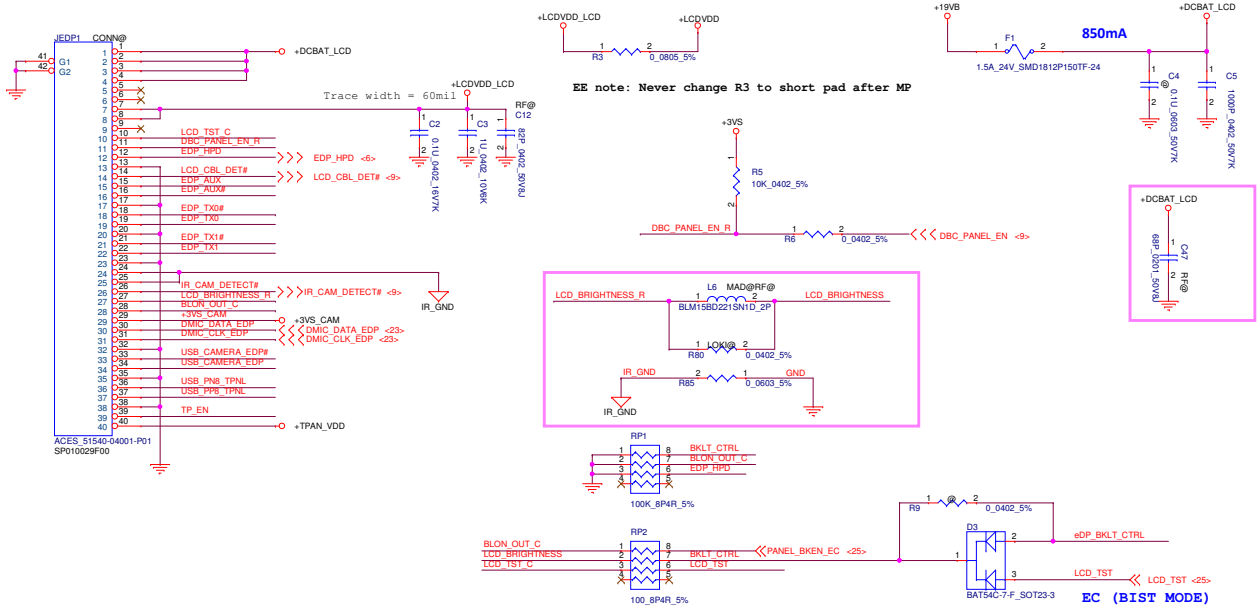
Title: **Finger Print**

Size	Document Number	Rev
	LA-F115P	0.1

Date: Friday, July 28, 2017 | Sheet 27 of 65

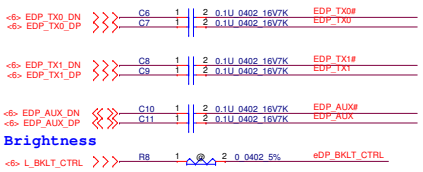
Main Func = LCD

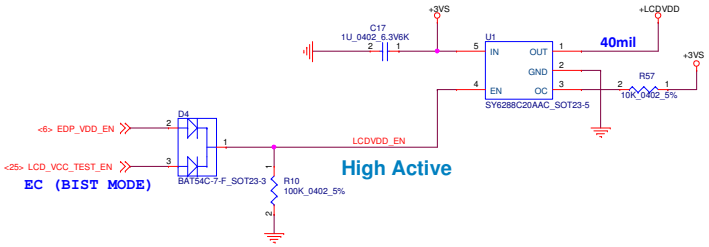
INVERTER POWER

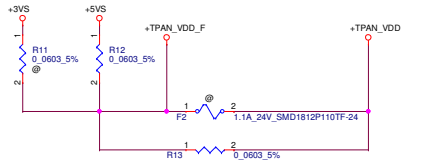


EE note: Never change R3 to short pad after MP

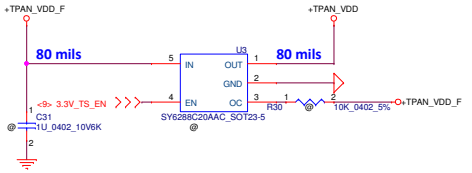
EC (BIST MODE)

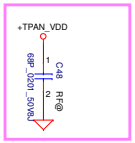






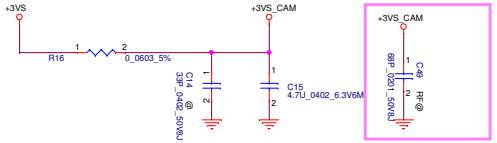
EE note: Never change R12/R13 to short pad after MP

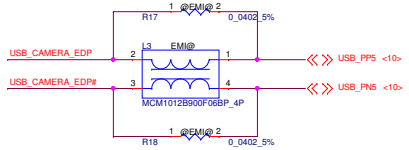




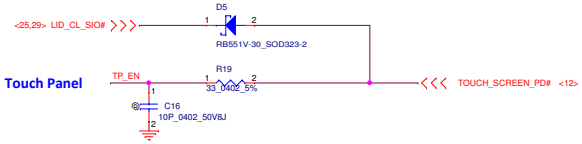
Main Func = CAM

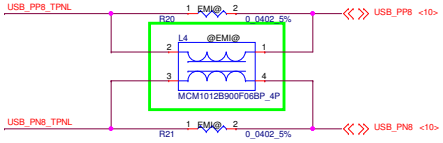
EE note: Never change R16 to short pad after MP

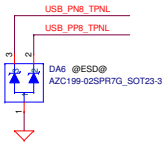




Main Func = TS







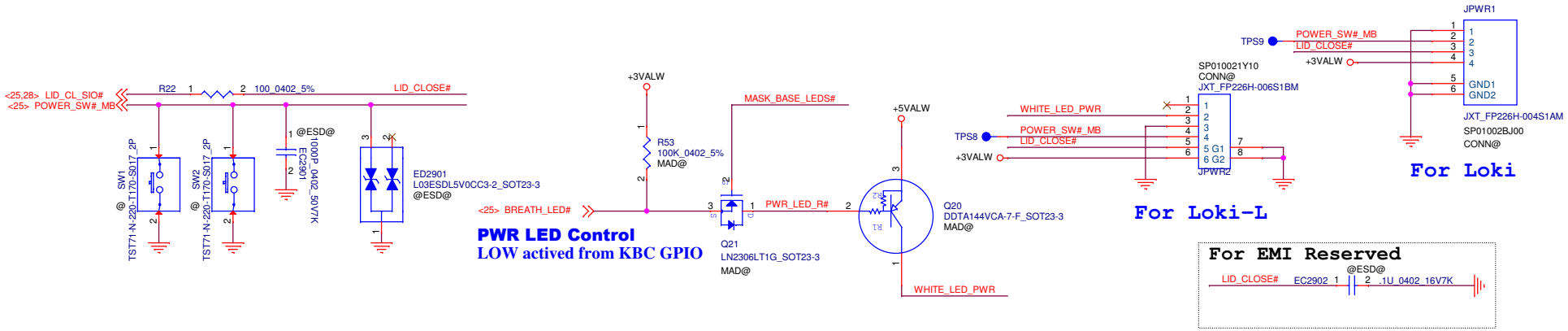
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	LCD/Cam/MIC/T.Panel		
Document Number	LA-F115P		Rev 0.1
Date: Friday, July 28, 2017	Sheet 28 of 65		

Main Func = Power BTN

Main Func = PWR LED

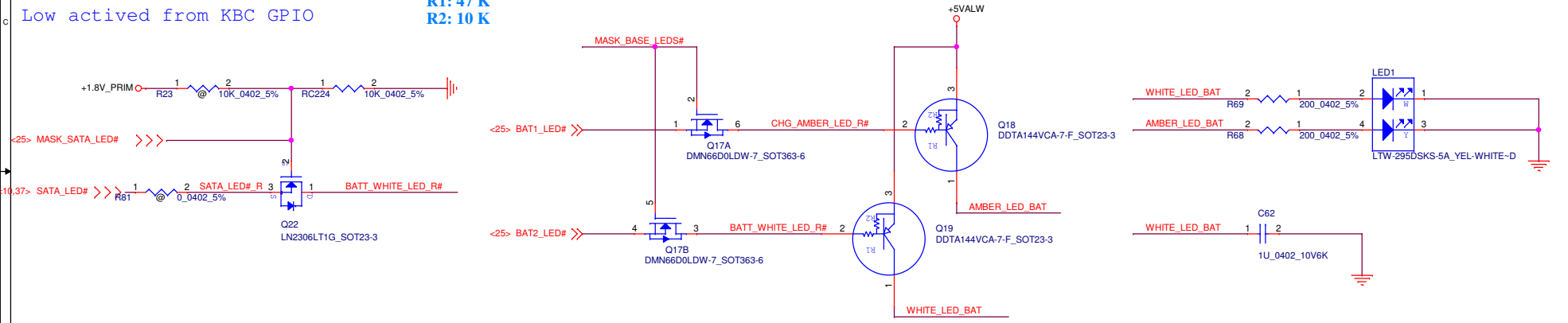
Low actived from KBC GPIO



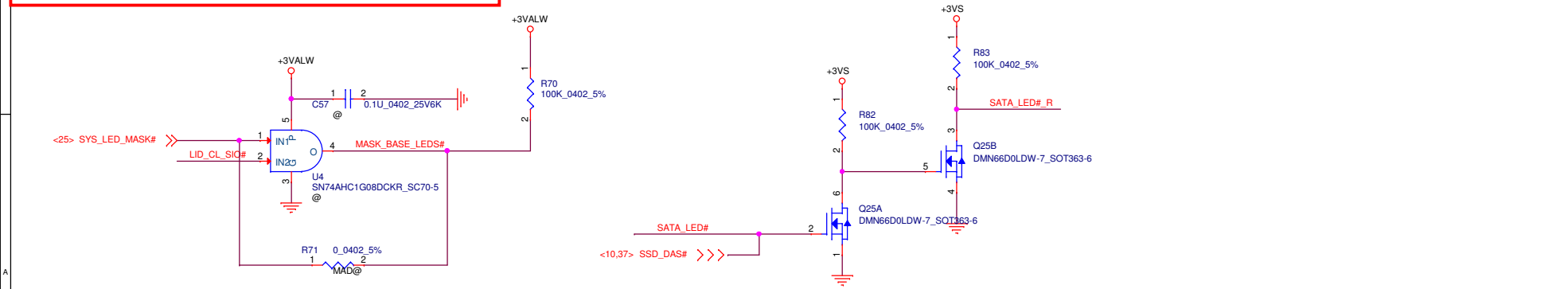
Main Func = Battery LED

Low actived from KBC GPIO

BJT
R1: 47 K
R2: 10 K



Main Func = Unobtrusive Mode



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

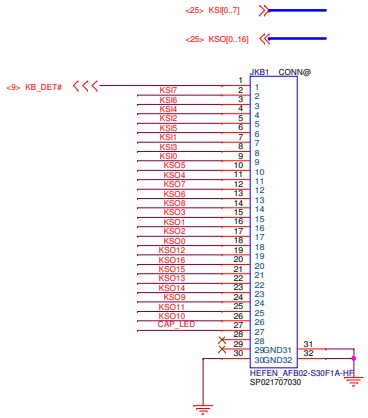
Compal Electronics, Inc.

Title: LED Board/Power Button

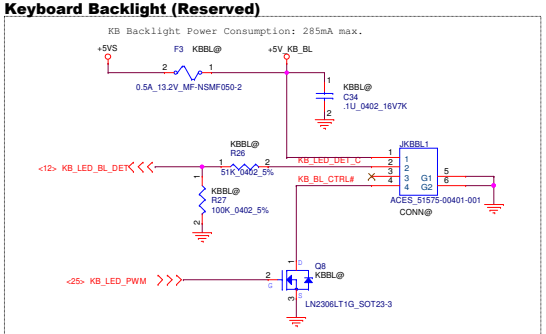
Size | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 29 of 65

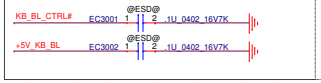
Main Func = KB



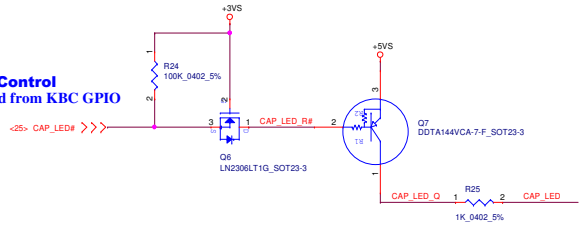
Keyboard Backlight (Reserved)



For EMI Reserved

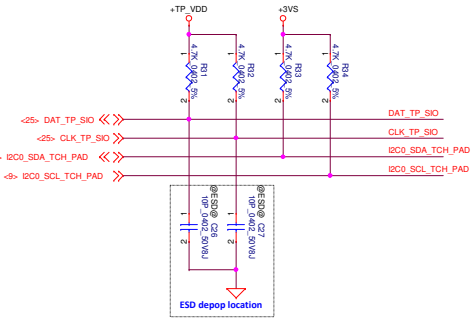


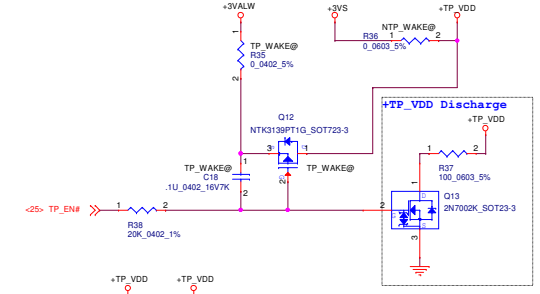
CAP LED Control
LOW actived from KBC GPIO

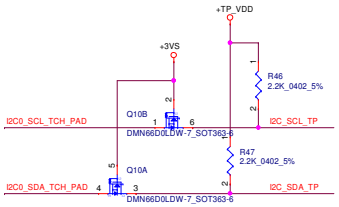


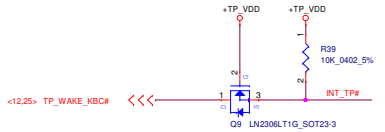
Main Func = TPAD

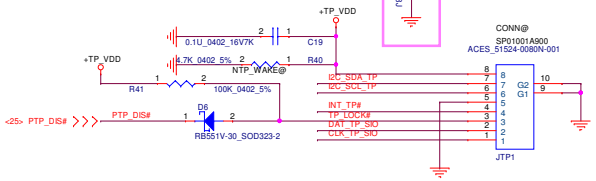
EC/PS2
PCH/I2C



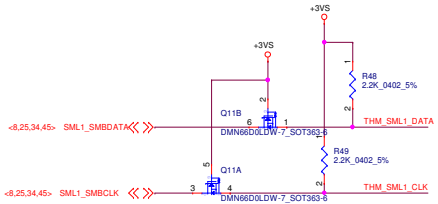


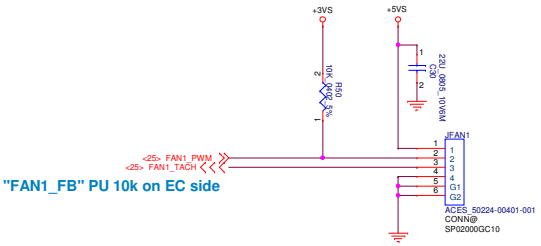




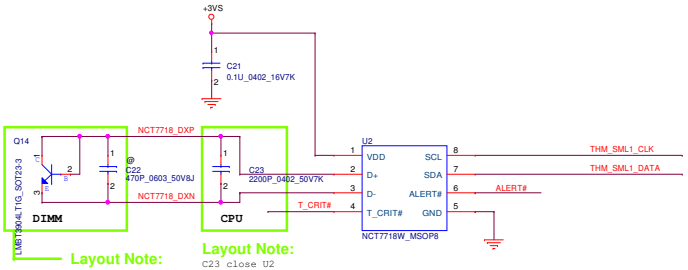


Main Func = Thermal





"FAN1_FB" PU 10k on EC side



Layout Note: DXN and DXP routing width and spacing is 10 mil / 10 mil.

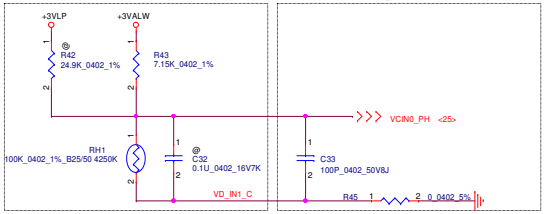
Layout Note: C23 close U2

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Main Func = OTP

Close to Thermal sensor

Close to KBC VD_IN1 for system thermal sensor



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

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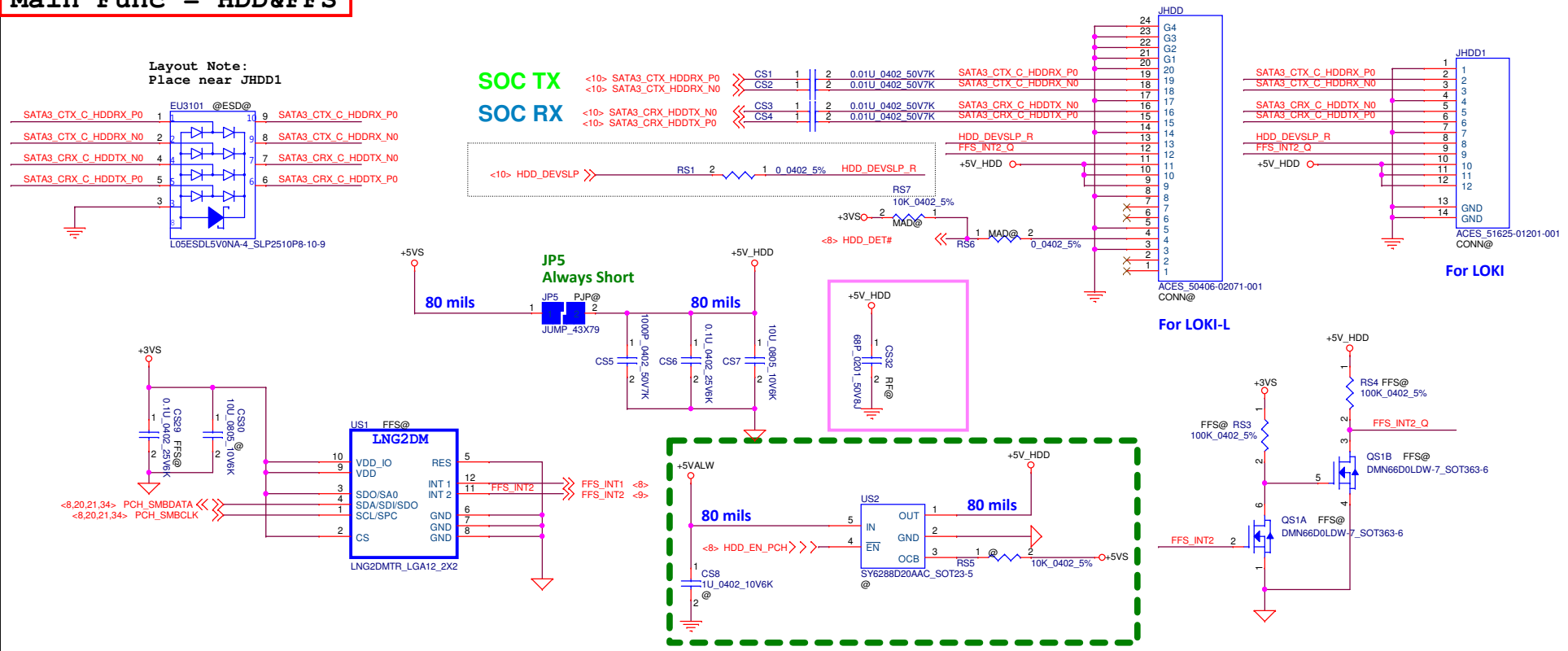
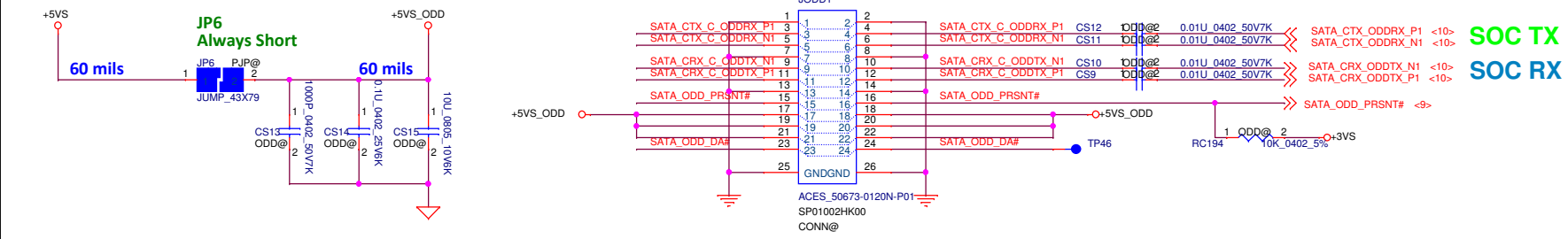
Compal Electronics, Inc.			
Title	Keyboard/Touch Pad/Thermal/FAN		
Size	Document Number	Rev	
	LA-F115P	0.1	
Date: Friday, July 28, 2017	Sheet 30 of 65		

Main Func = HDD&FFS



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	

Main Func = ODD



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
PRSNT	P1	8
5V	P2	9
5V	P3	10 11
Attention	P4	12
GND	P5	
GND	P6	

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

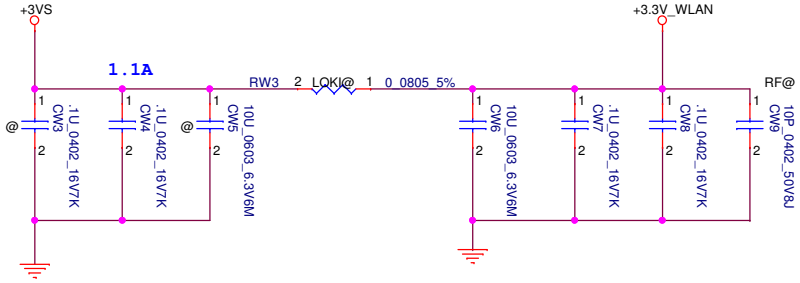
Title: HDD/FFS/ODD

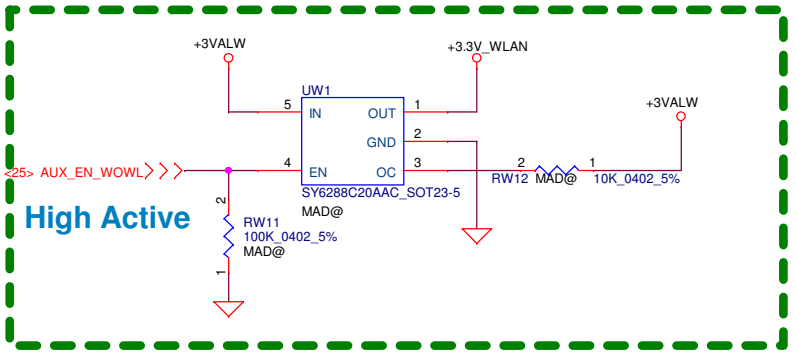
Size: Custom | Document Number: LA-F115P | Rev: 0.1

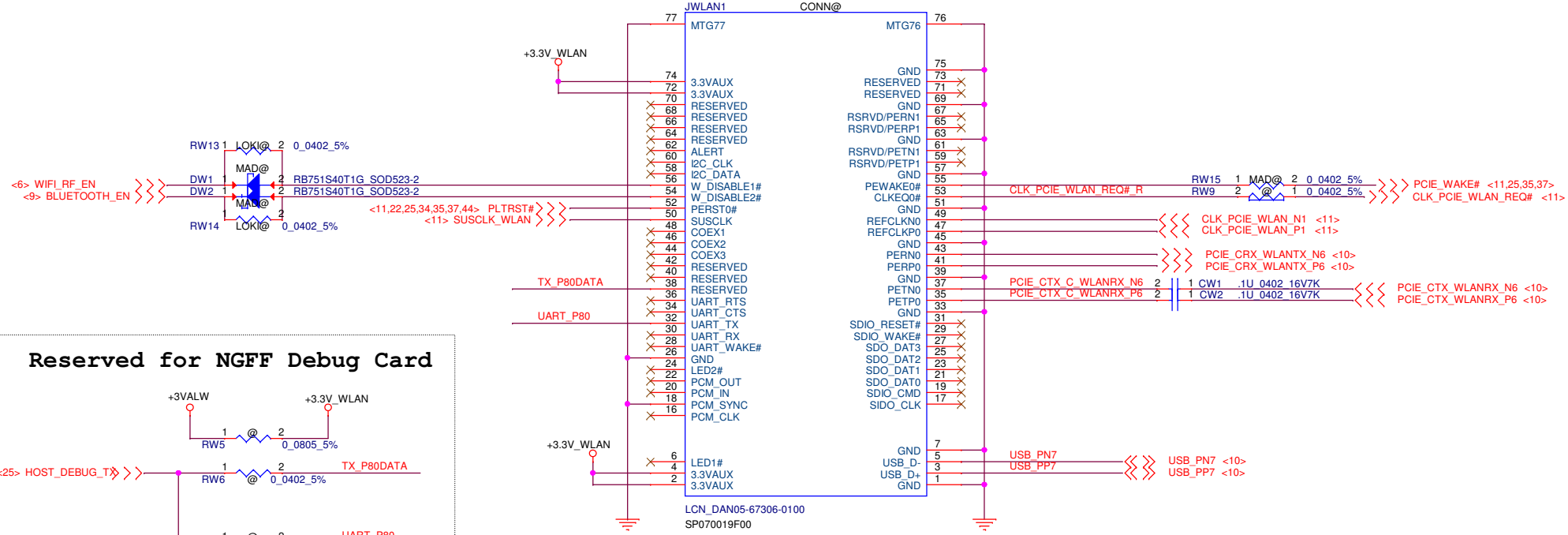
Date: Friday, July 28, 2017 | Sheet 31 of 65

Main Func = WLAN

A Key CONN







Reserved for NGFF Debug Card

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: NGFF_WLAN CONN

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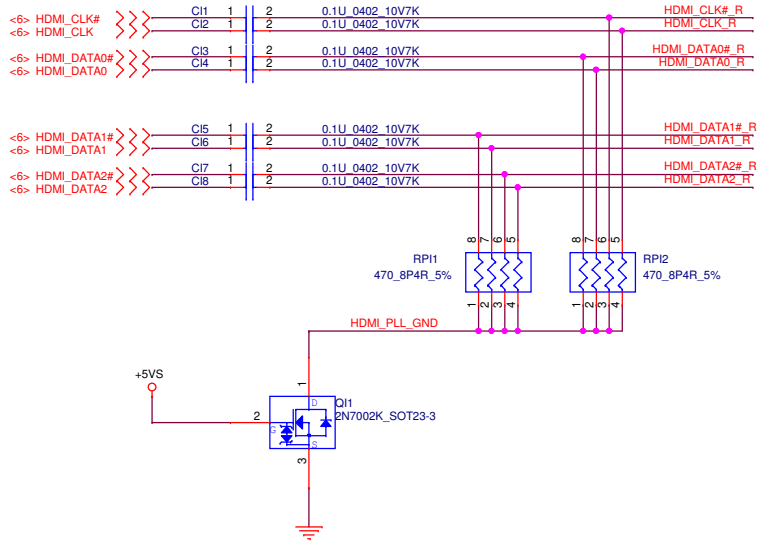
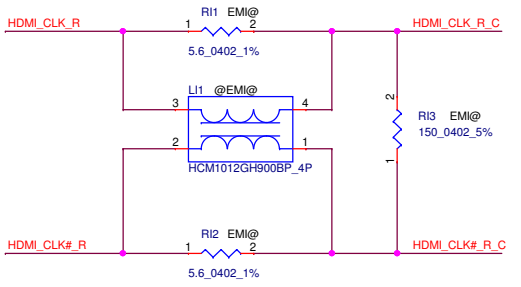
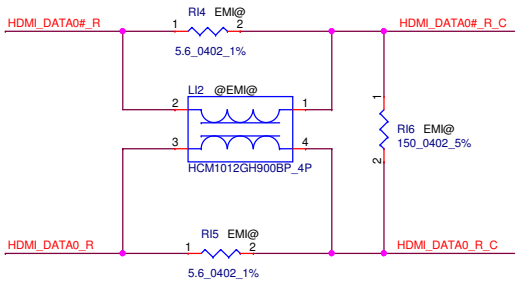
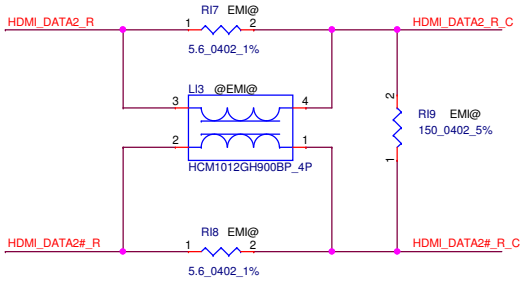
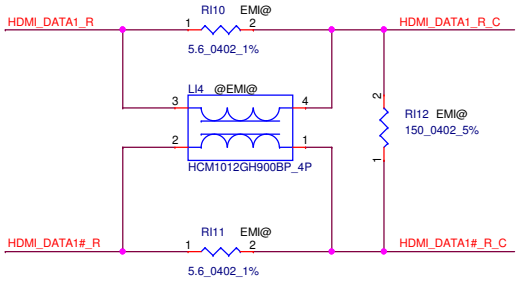
Main Func = HDMI

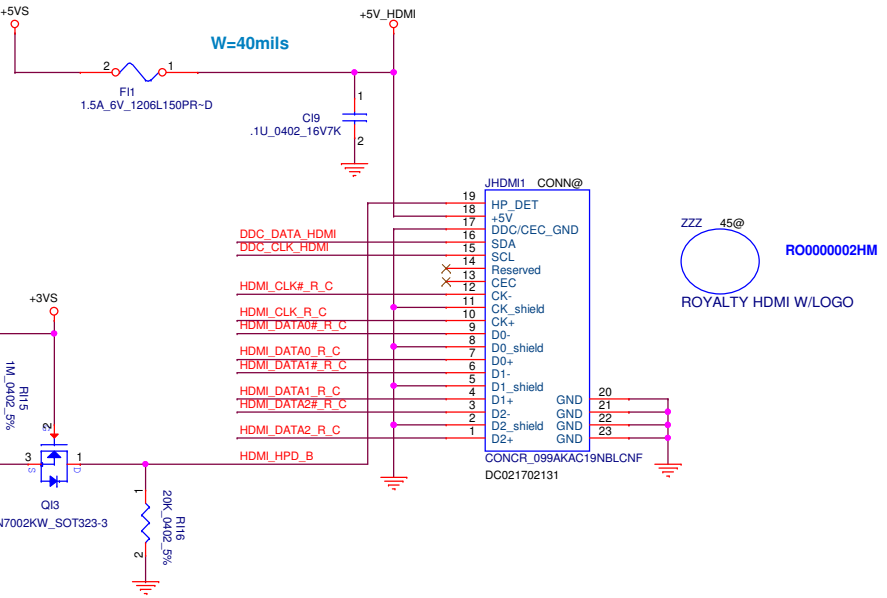


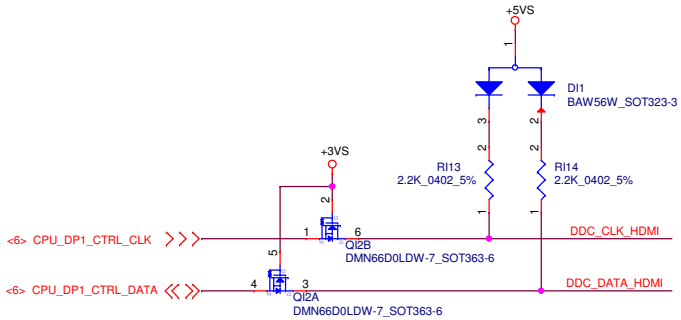












Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: HDMI L.Shifter/Conn

Size: | Document Number: LA-F115P | Rev: 0.1

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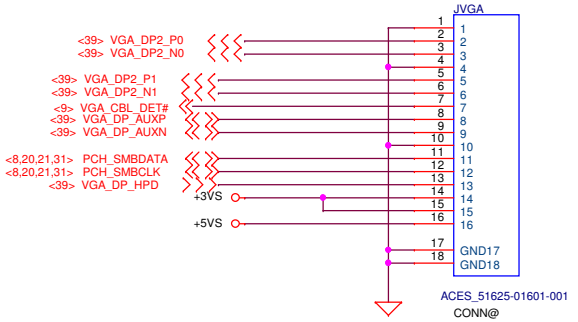
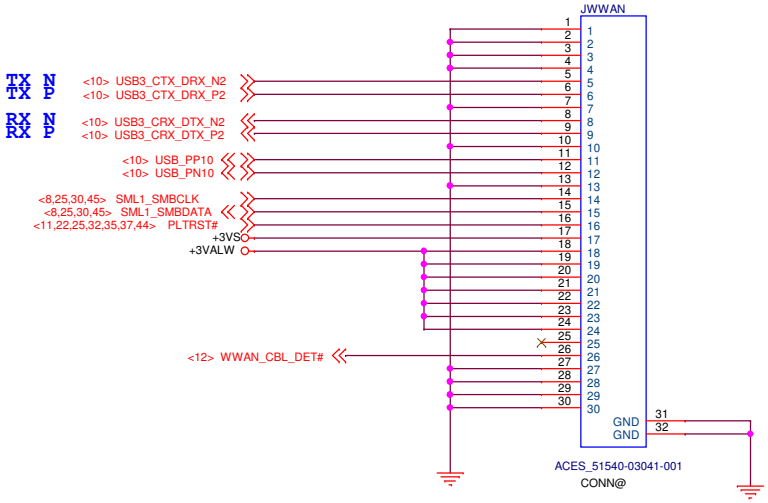
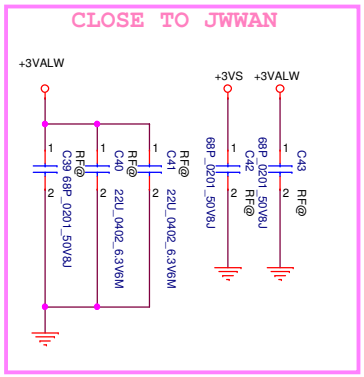
Main Func = WWAN/B & VGA/B







RTL8111G-CGT (71.08111.U03/LDO Mode): 10/100/1000M < 252 mW.
RTL8106E-CG (071.08106.0003): 10/100M <70mW.

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: IO_DB(WWAN/VGA)			
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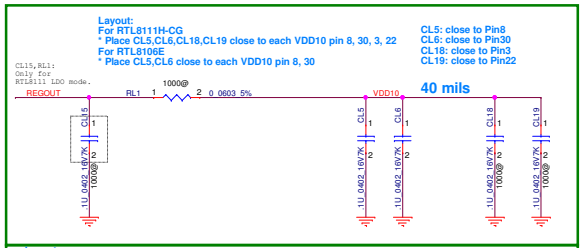
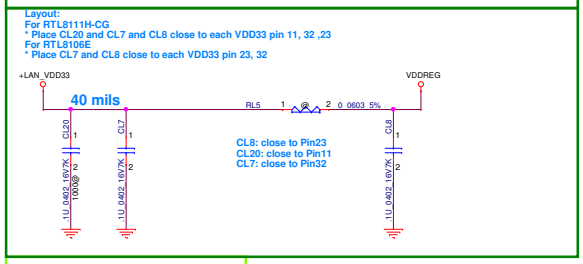
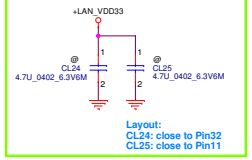
Main Func = LAN

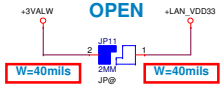
LAN Chip (10/100/1000M & 10/100M co-layout)

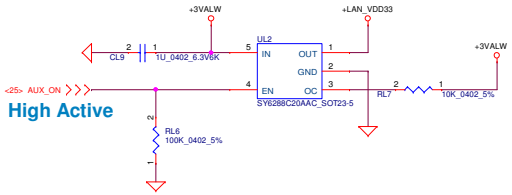


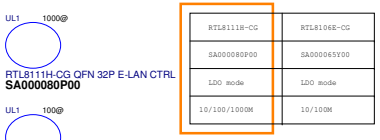


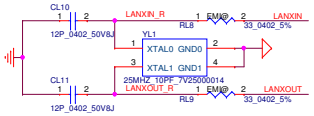


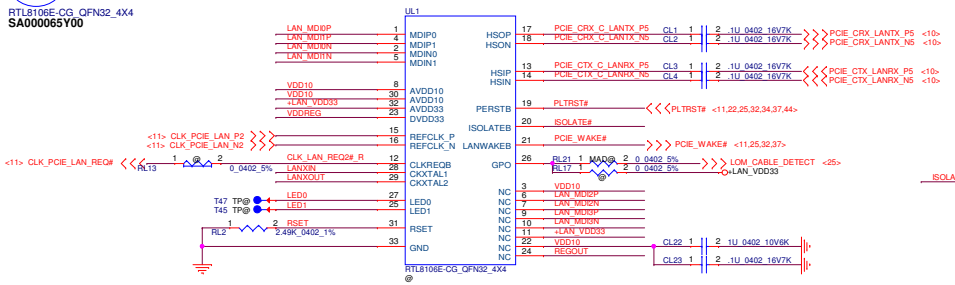
+LAN_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.



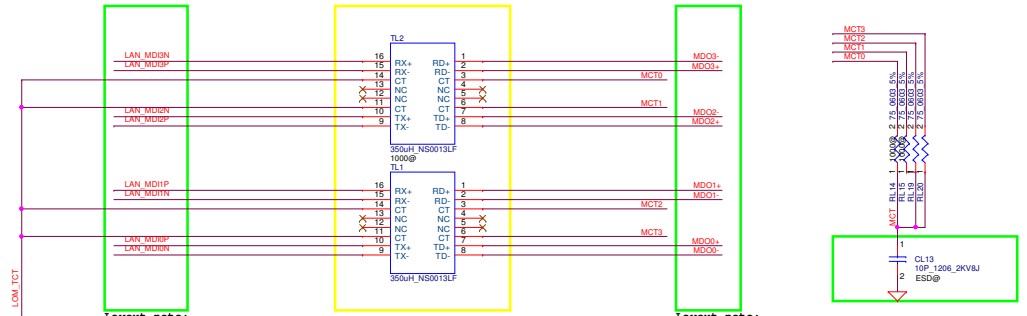




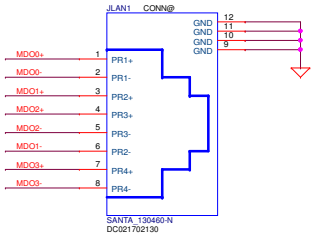




LAN TransFormer (10/100/1000M & 10/100M co-layout)



	1.0V Source	RL1	CL15	CL18	CL19	CL20	CL8
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

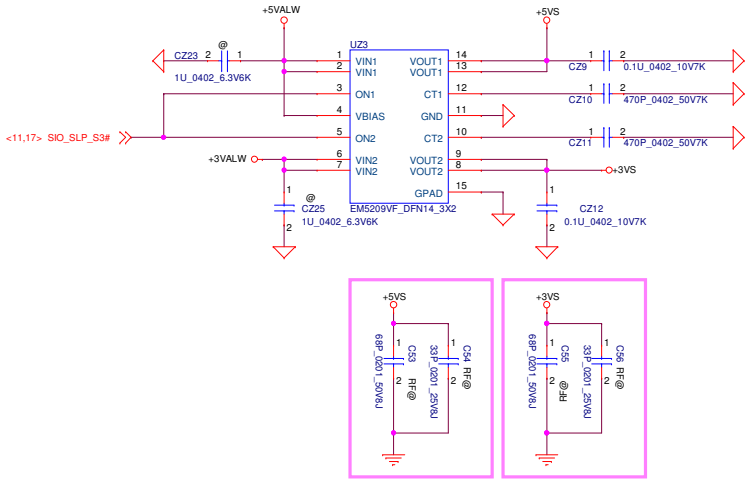


Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.	
Title	P35-LAN RTL8111/RTL8106
Size	Document Number: LA-F115P — Rev: 0.1
Date: Friday, July 28, 2017	Sheet 35 of 65

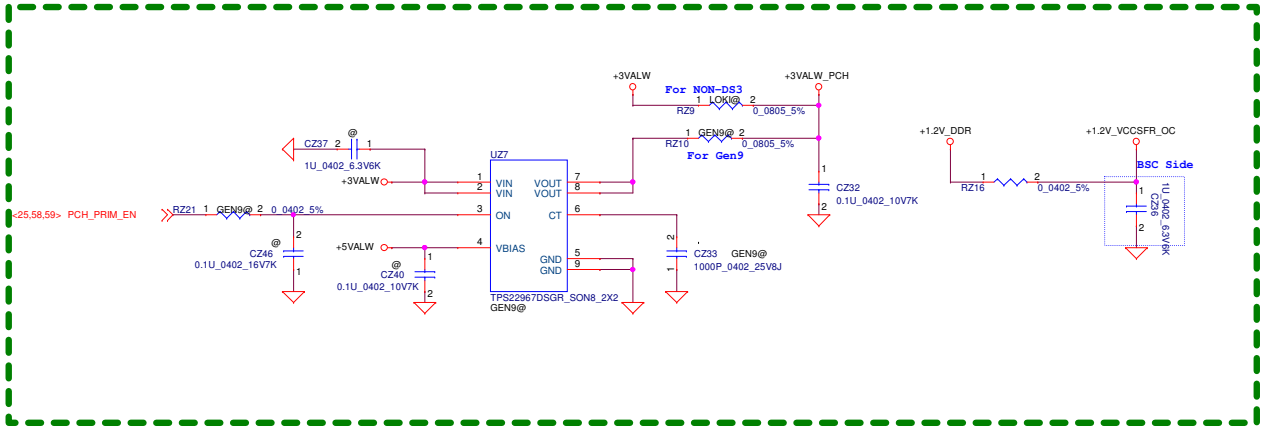
Main Func = DC/DC

+5VS/+3VS for System



+3VALW_PCH for System
+1.2V_DDR TO +1.2V_VCCSFR_OC

NON-DSX(LOKI)
DSX(LOKI-L)



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: DC/DC

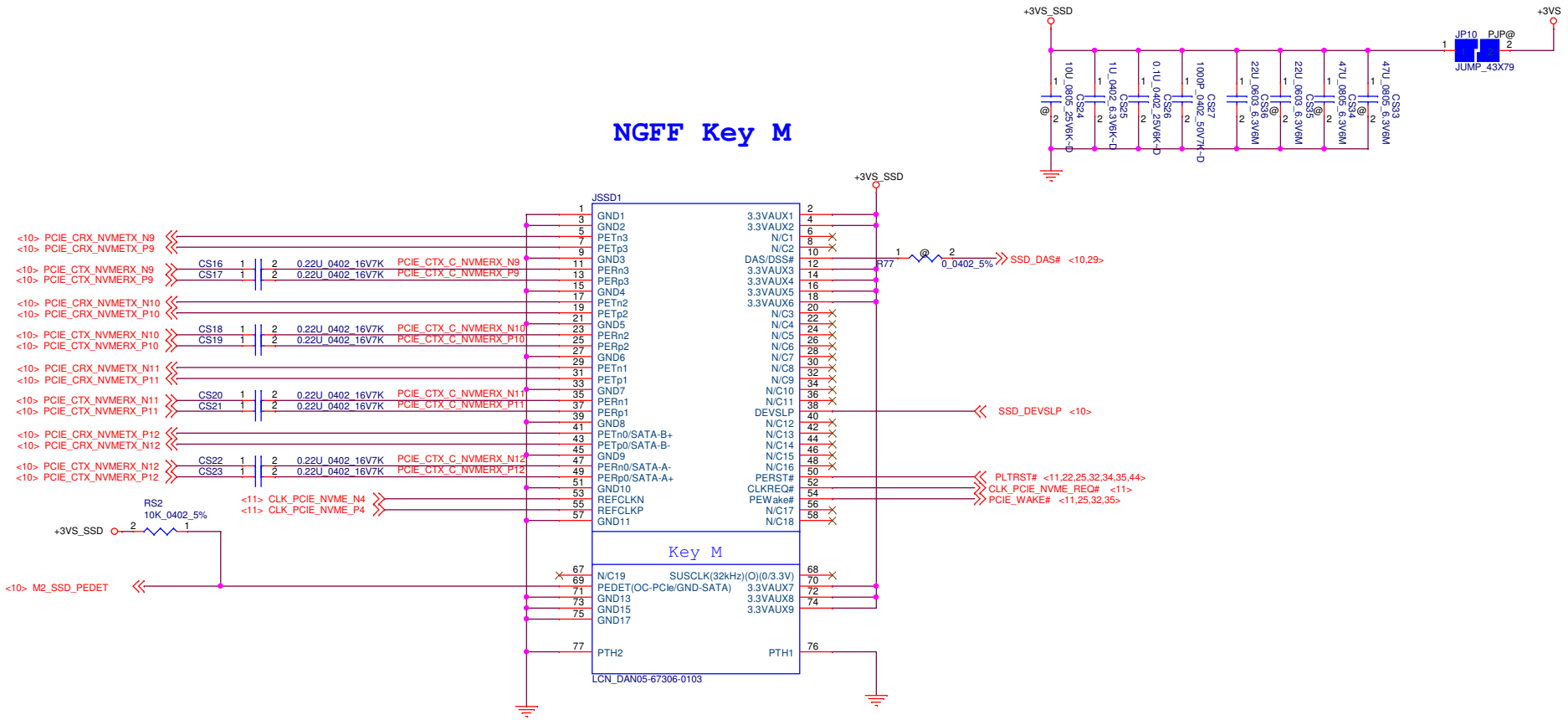
Size | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 36 of 65

Main Func = SSD

M Key CONN

NGFF Key M



PEDET	Module Type
0	SATA
1	PCIE

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: NVME SSD

Size | Document Number: LA-F115P | Rev: 0.1

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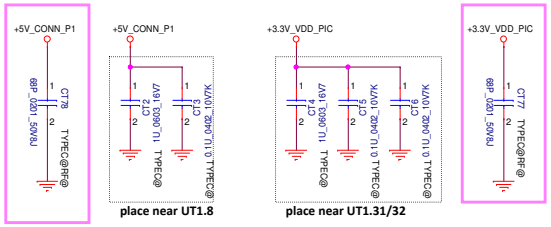
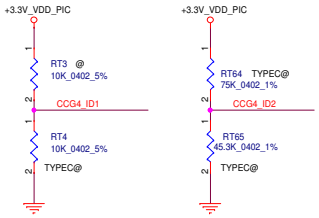
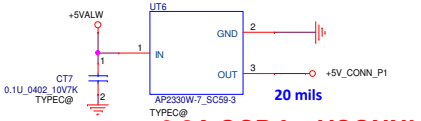
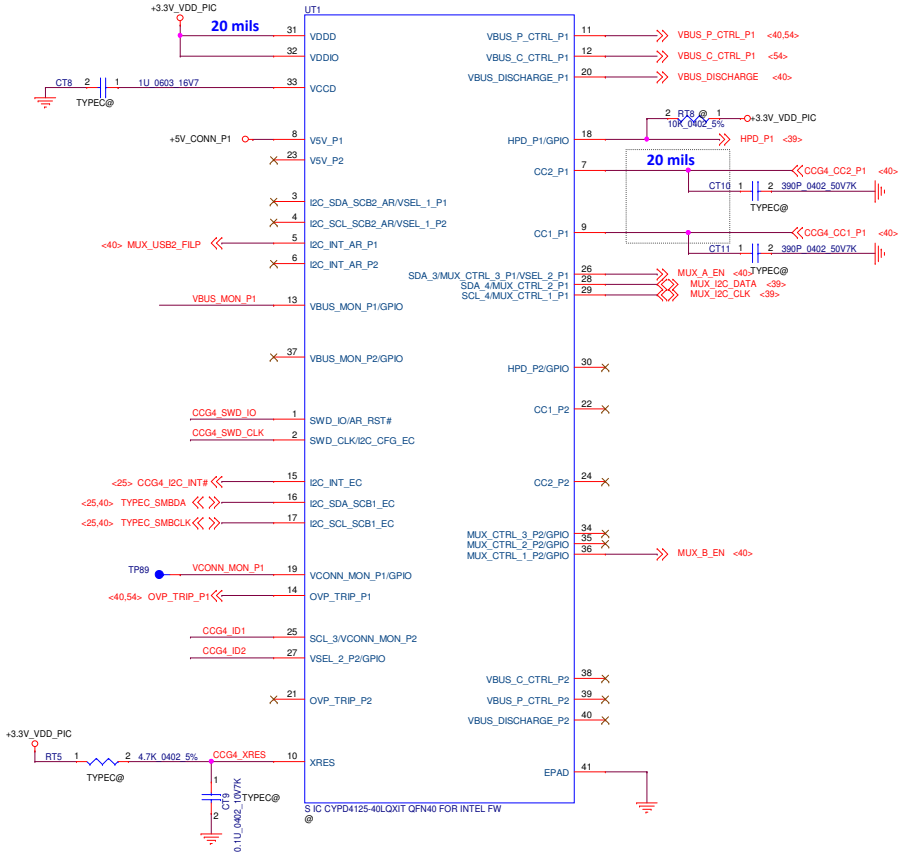
Main Func = CCG4

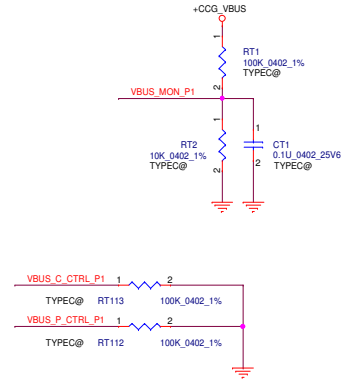


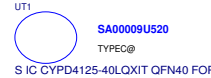


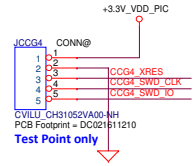


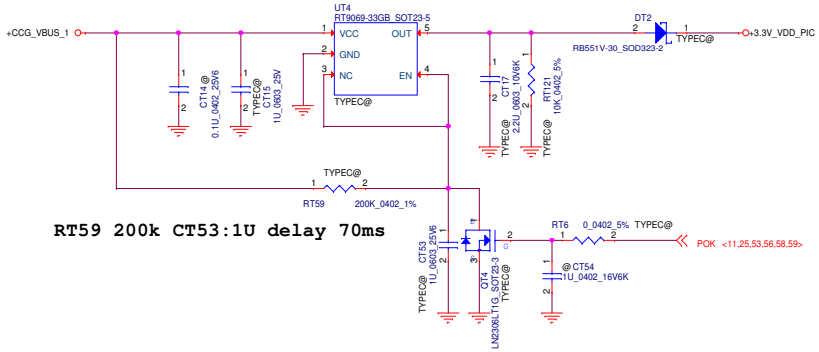
0.2A OCP for VCONN!











Voltages for various platform on "CCG4_ID_1" pin and "CCG4_ID_2" pin

#	Platform	Voltage on CCG4_ID_1	Voltage on CCG4_ID_2
1	Single Port - Intel - DDM support - Armani 13" & 14"	L0	L7
2	Single Port - Intel - DDM support - Kyloren	L0	L6
3	Single Port - Intel - DDM support - Miyake	L0	L5
4	Single Port - Intel - DDM support - Loki 13"	L0	L4
5	Single Port - Intel - DDM support - Loki 15" & 17" (Motherboard is same)	L0	L3
6	Single Port - Intel - DDM support - StarLord KBL - R	L0	L2
7	Single Port - AMD - DDM not supported - Loki 15" & 17" (Motherboard is same)	L4	L0

Voltage level	Voltage value
L0	0V
L1	3.3V
L2	3.3V/2
L3	3.3V/3
L4	3.3V/4
L5	3.3V/5
L6	3.3V/6
L7	3.3V/7

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: Cypress PD Control

Size | Document Number: LA-F115P | Rev: 0.1

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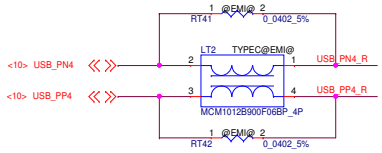
Main Func = typec MUX & DP MUX

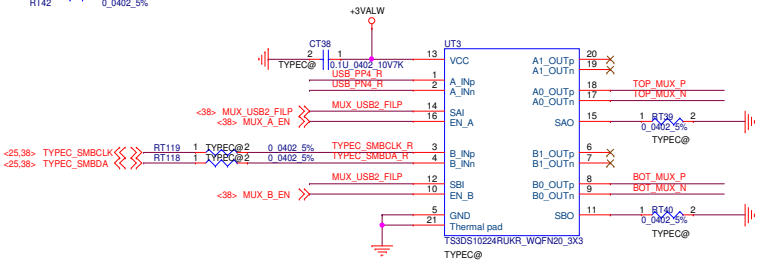
Table 8-7 TUSB546 Receiver Equalization GPIO Control

USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Port			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @5GHz (dB)	SSEQ1 pin Level	SSEQ0 pin Level	EQ GAIN @5GHz (dB)	DPEQ1 pin Level	DPEQ0 pin Level	EQ GAIN @5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	F	10	F	F	10	F	F	10
F	1	11	F	1	11	F	1	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15

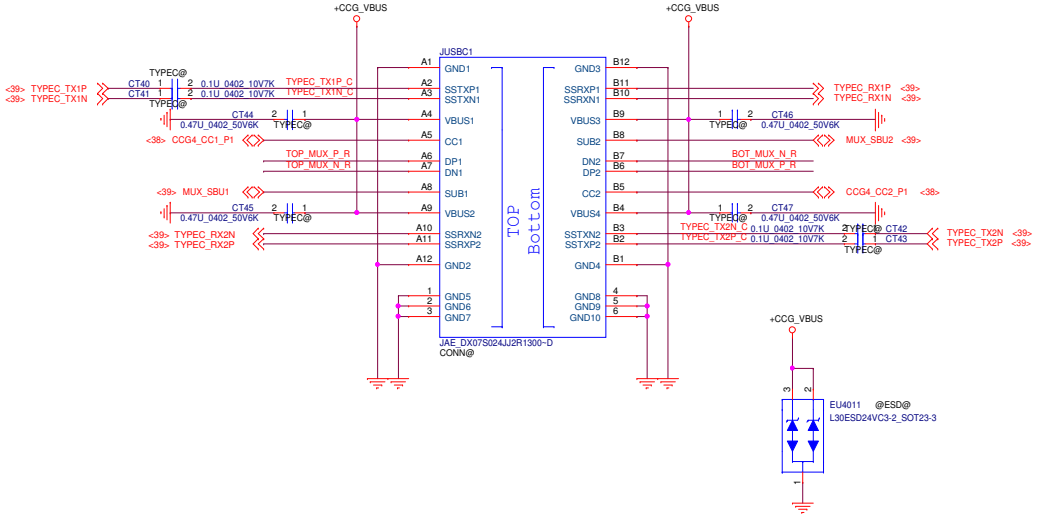
Main Func = USB2/I2C Mux

Close to JUSBC1 <500mil

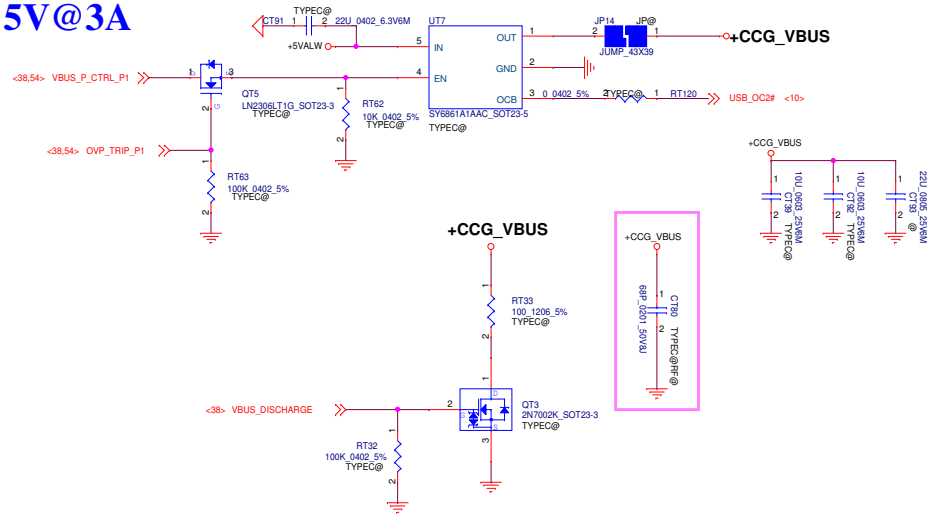


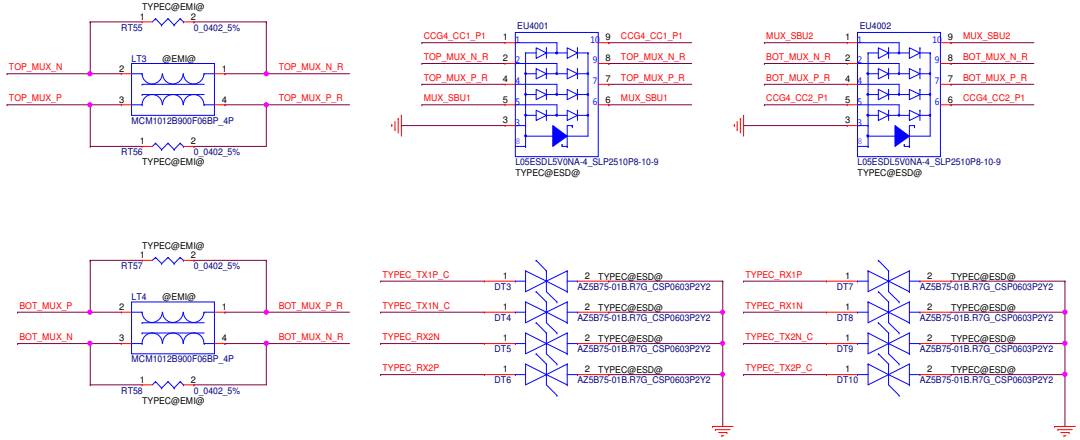


MUX_USB2_FILP	MUX_A_EN	MUX_B_EN	A0_OUT	B0_OUT
0	0	1	--	USB2
0	1	1	I2C	USB2
1	1	0	USB2	--
1	1	1	USB2	I2C



5V@3A





Type-C 5V Provide Path Control

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Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: TYPE-C

Size | Document Number: LA-F115P | Rev: 0.1

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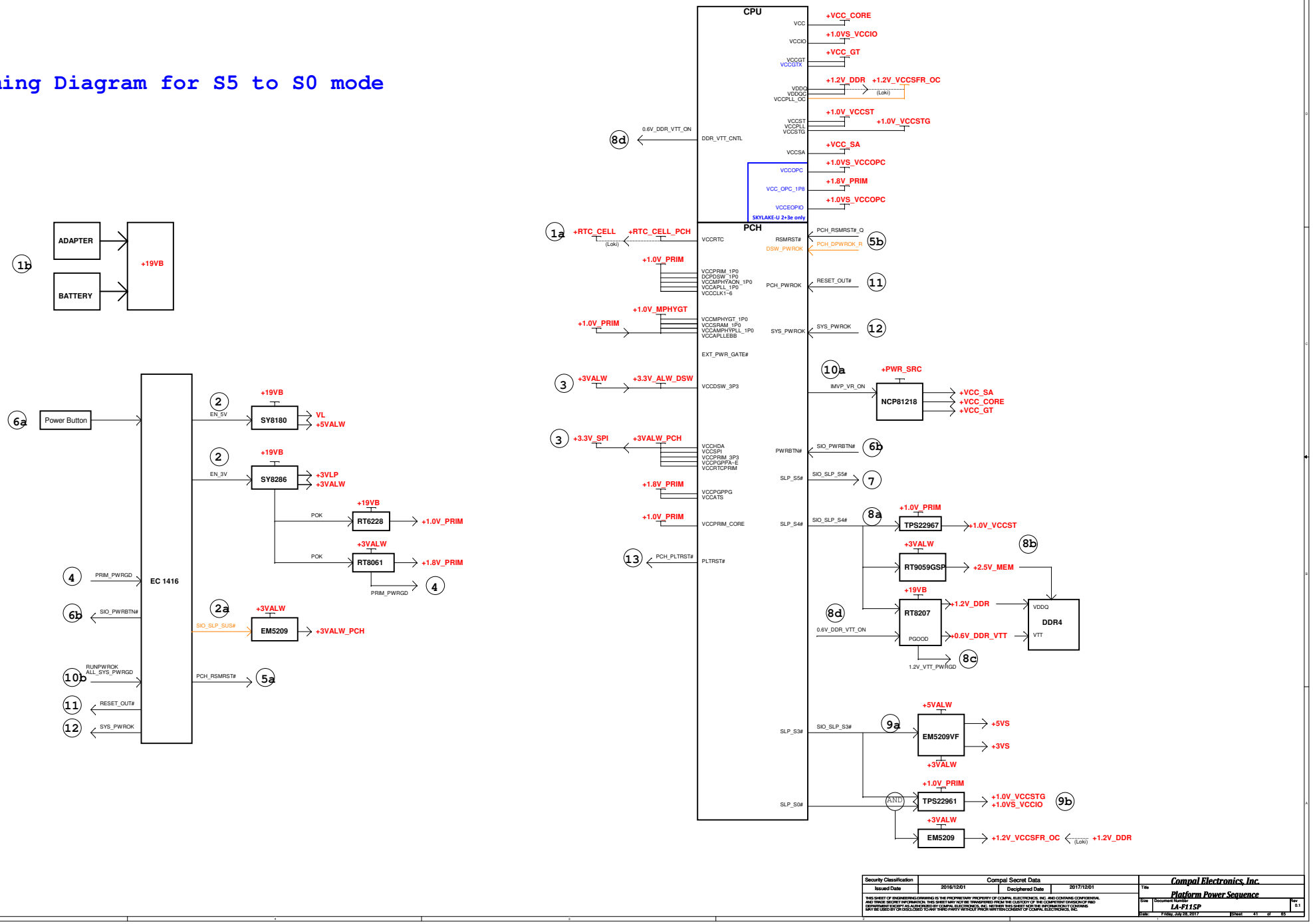
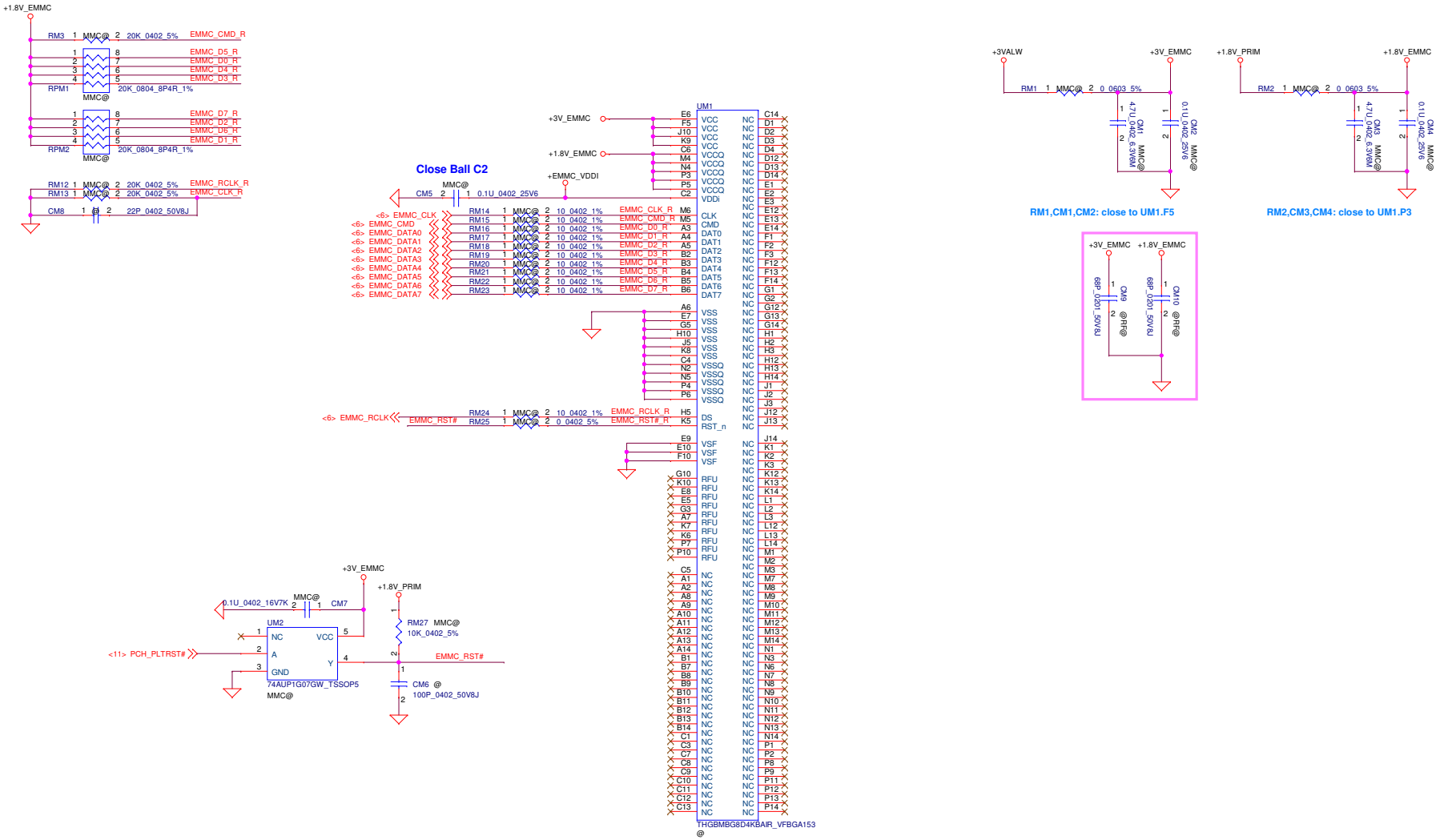
Timing Diagram for S5 to S0 mode



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/12/01	Deciphered Date	2017/12/01
Title	Platform Power Sequence		
Size	Document Number		Rev
	LA-F115P		0.1
Date: Friday, July 28, 2017	Sheet 41 of 65		

Main Func = eMMC



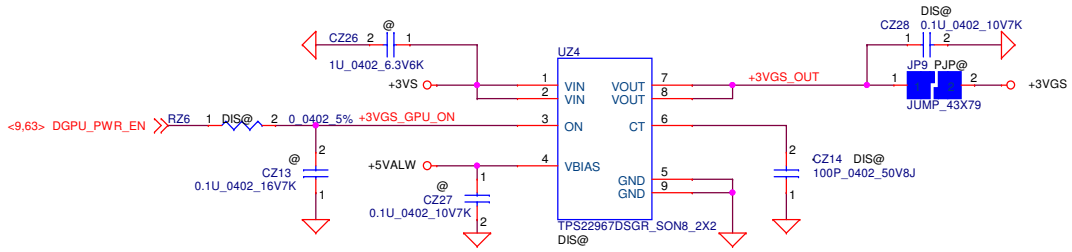
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.		
Title: RAV for eMMC		
Size	Document Number: LA-F115P	Rev: 0.1
Date: Friday, July 28, 2017	Sheet 42 of 65	

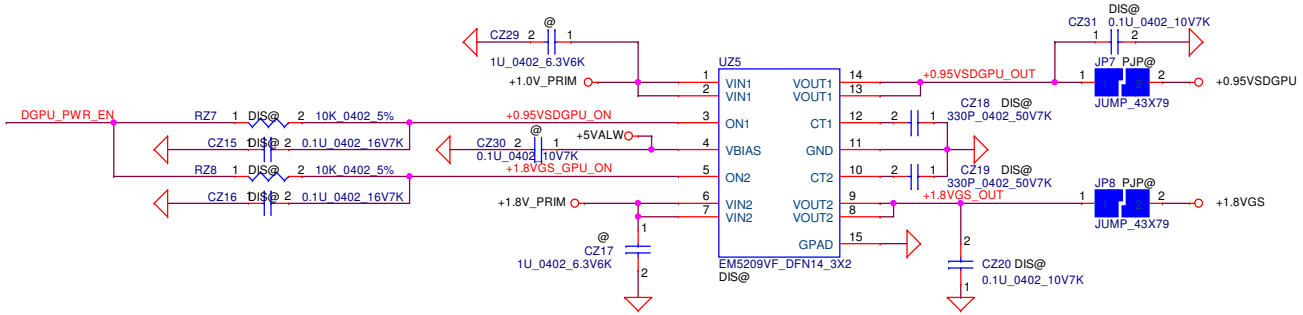
Main Func = GPU

+3V/+0.95V/+1.8V for GPU

Maximum Output Current 4A



250mA
JP9
Always Short



2300mA
JP7
Always Short

500mA
JP8
Always Short

Maximum Output Current 6A

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

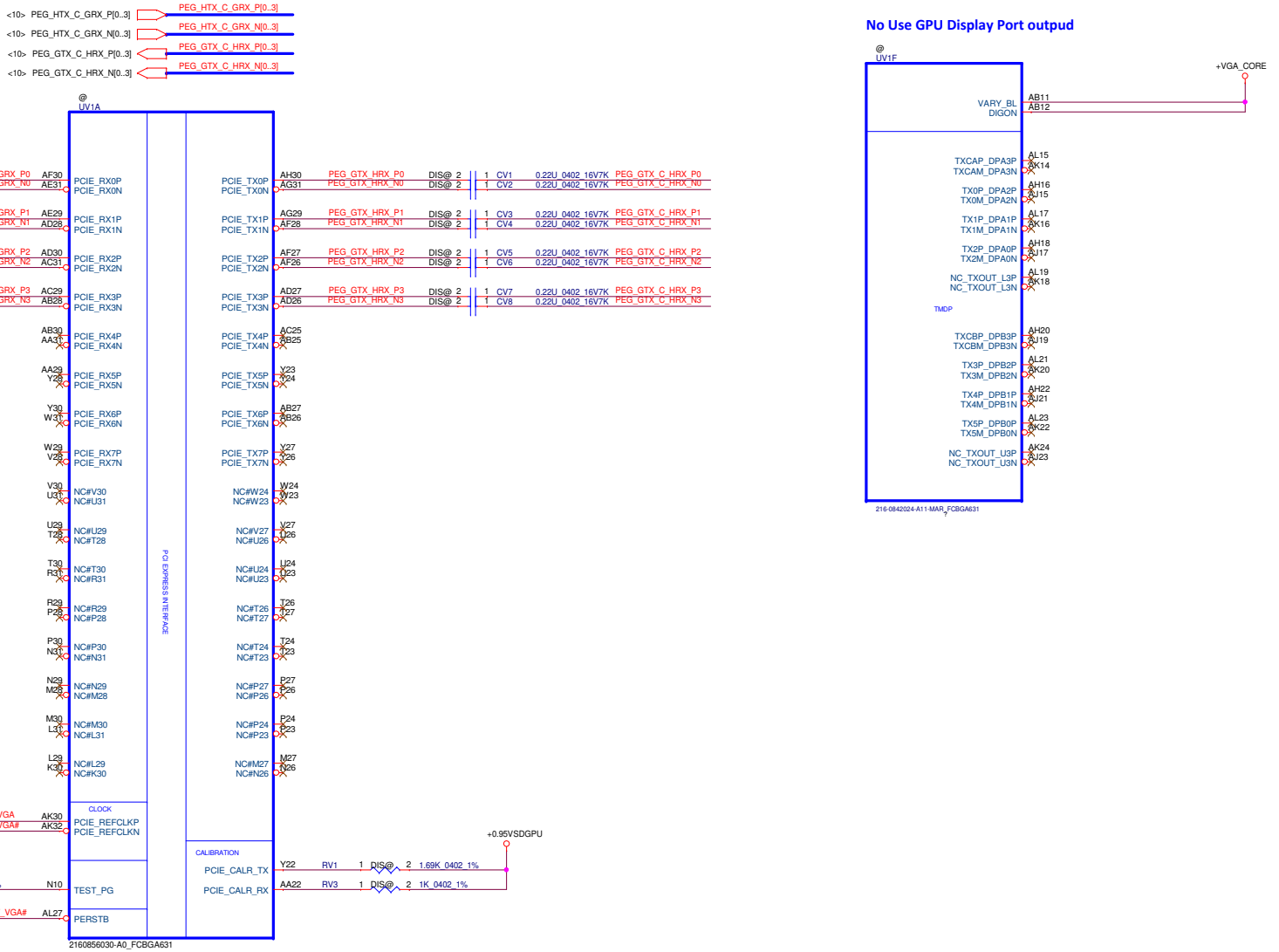
Compal Electronics, Inc.

Title: **GPU Power**

Size | Document Number: **LA-F115P** | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 43 of 65

Main Func = GPU



GPU R1/R3

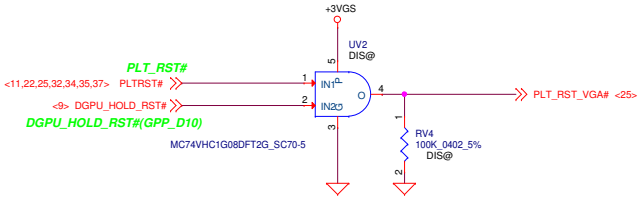
UV1 — SA0000B1W0L — M2_50@

S IC 216-0889004 A0 R17M-M2-50 FCBGA 0FD

UV1 — SA0000B1W1L — M2_50_R3@

S IC 216-0889004 A0 R17M-M2-50 WESTON XT BGA 631P GPU A31 !

No Use GPU Display Port outpud



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: MESO_(1/5)_PCIE/DP

Size | Document Number: LA-F115P | Rev: 0.1

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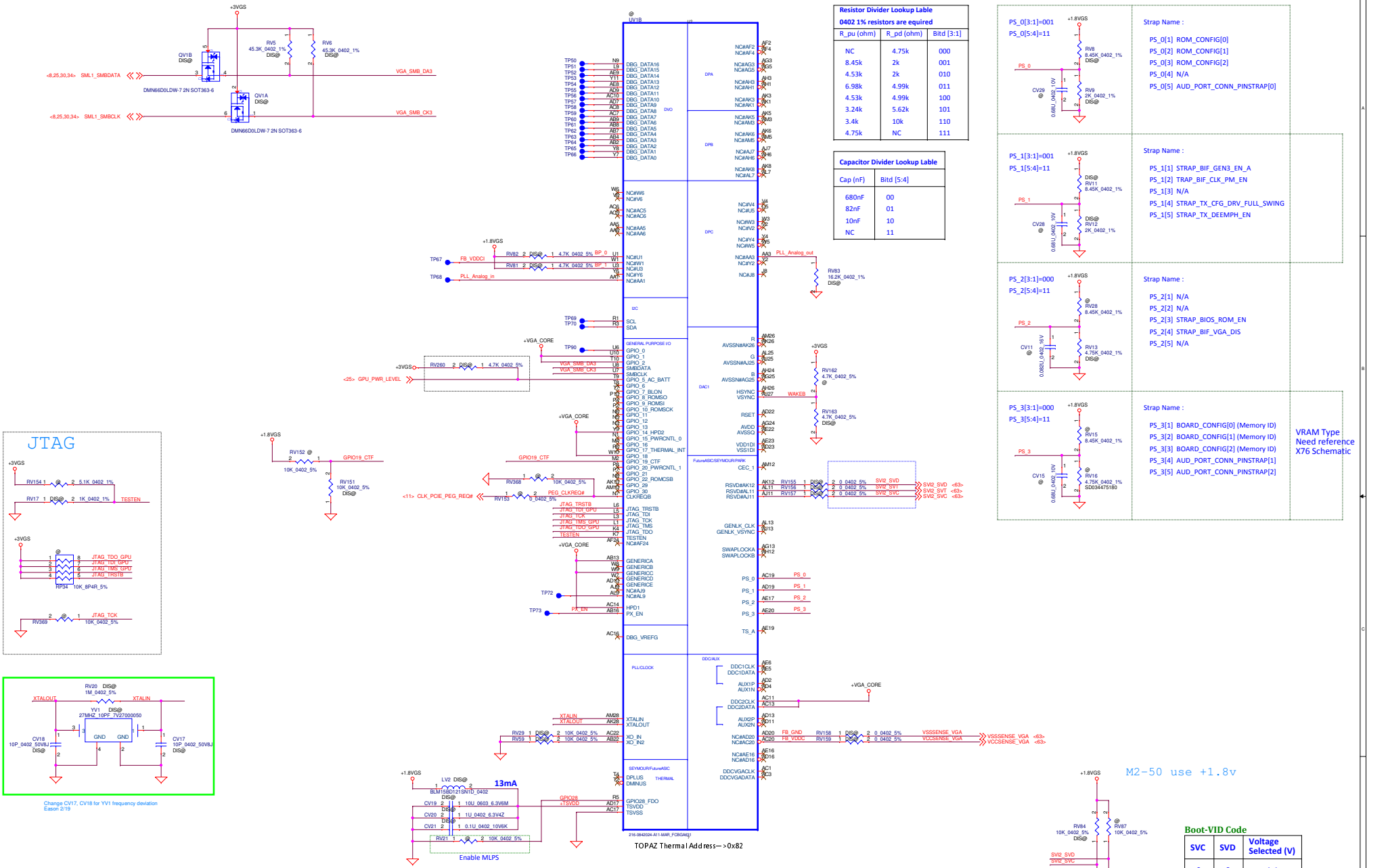
Main Func = GPU



Resistor Divider Lookup Lable

0402 1% resistors are equired

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

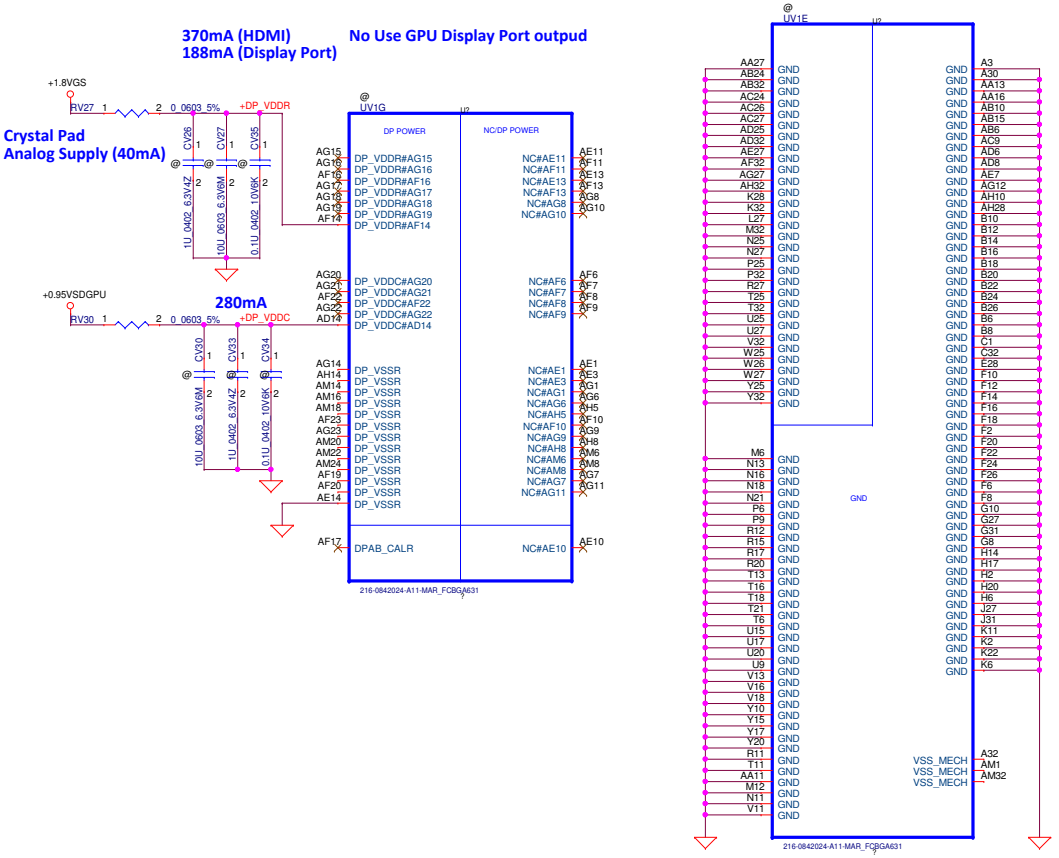
Compal Electronics, Inc.

Title: MESO_(2/5)_MSIC

Size: | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 45 of 65

Main Func = GPU



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: MESO_(3/5)_Power/GND

Size: | Document Number: LA-F115P | Rev: 0.1

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Main Func = GPU

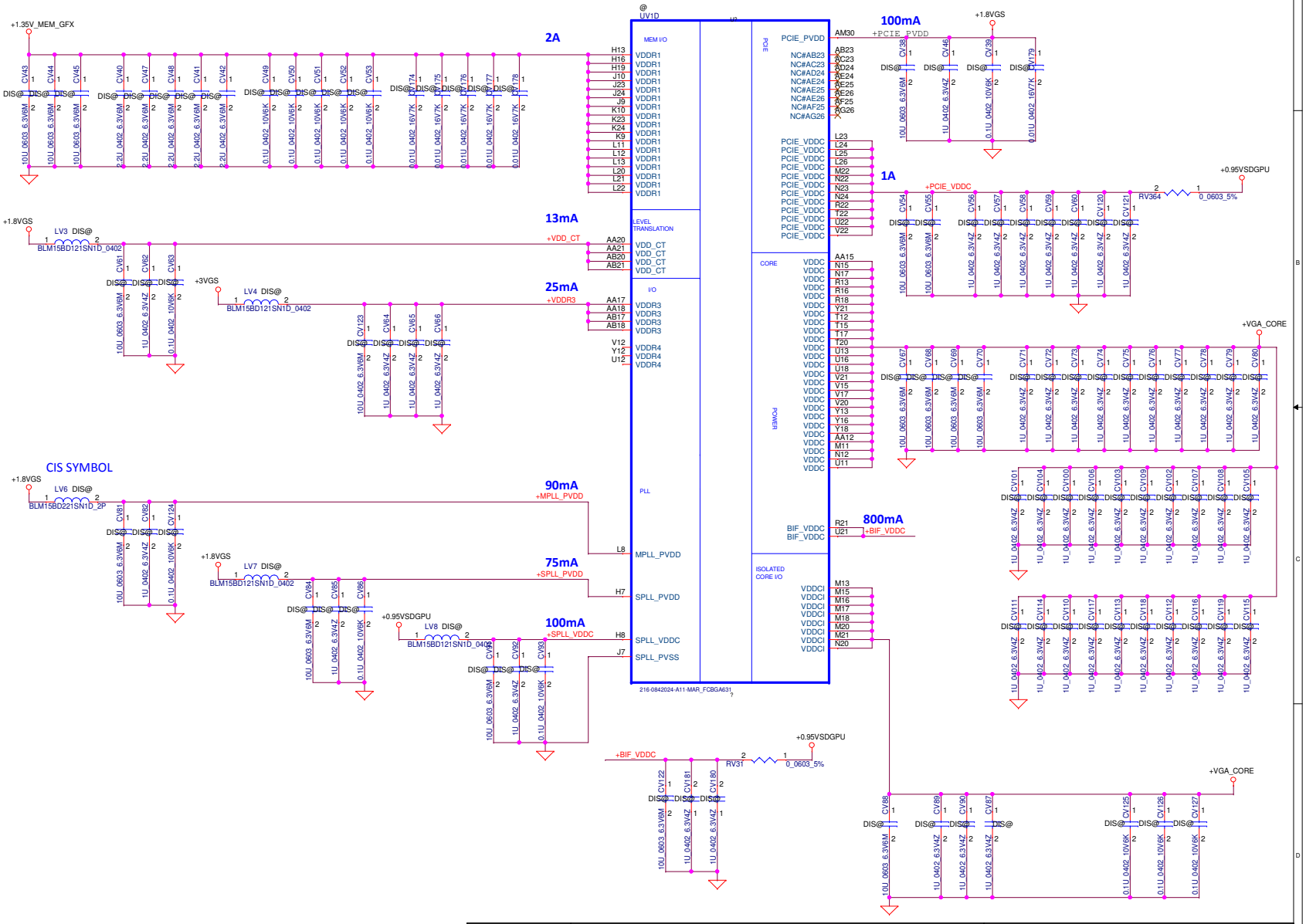
+VGA_CORE	10uF	1uF	0.1uF
VDDC	4	30	0
VDDCI	1	3	3

+0.95VSDGPU	10uF	1uF	0.1uF
PCIE_VDDC	2	7	0
BIF_VDDC	1	2	0
SPLL_VDDC	1	1	1
+DP_VDDC	0	0	0

+1.35V_MEM_GFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1	3	5	5	5

+1.8VGS	10uF	1uF	0.1uF
PCIE_PVDD	1	1	1
MPLL_PVDD	1	1	1
SPLL_PVDD	1	1	1
VDDR4 (NC)	0	0	0
VDD_CT	1	1	1
+TSVDD	1	1	1
+DP_VDDR	0	0	0

+3VGS	10uF	1uF	0.1uF
VDDR3	1	3	0



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

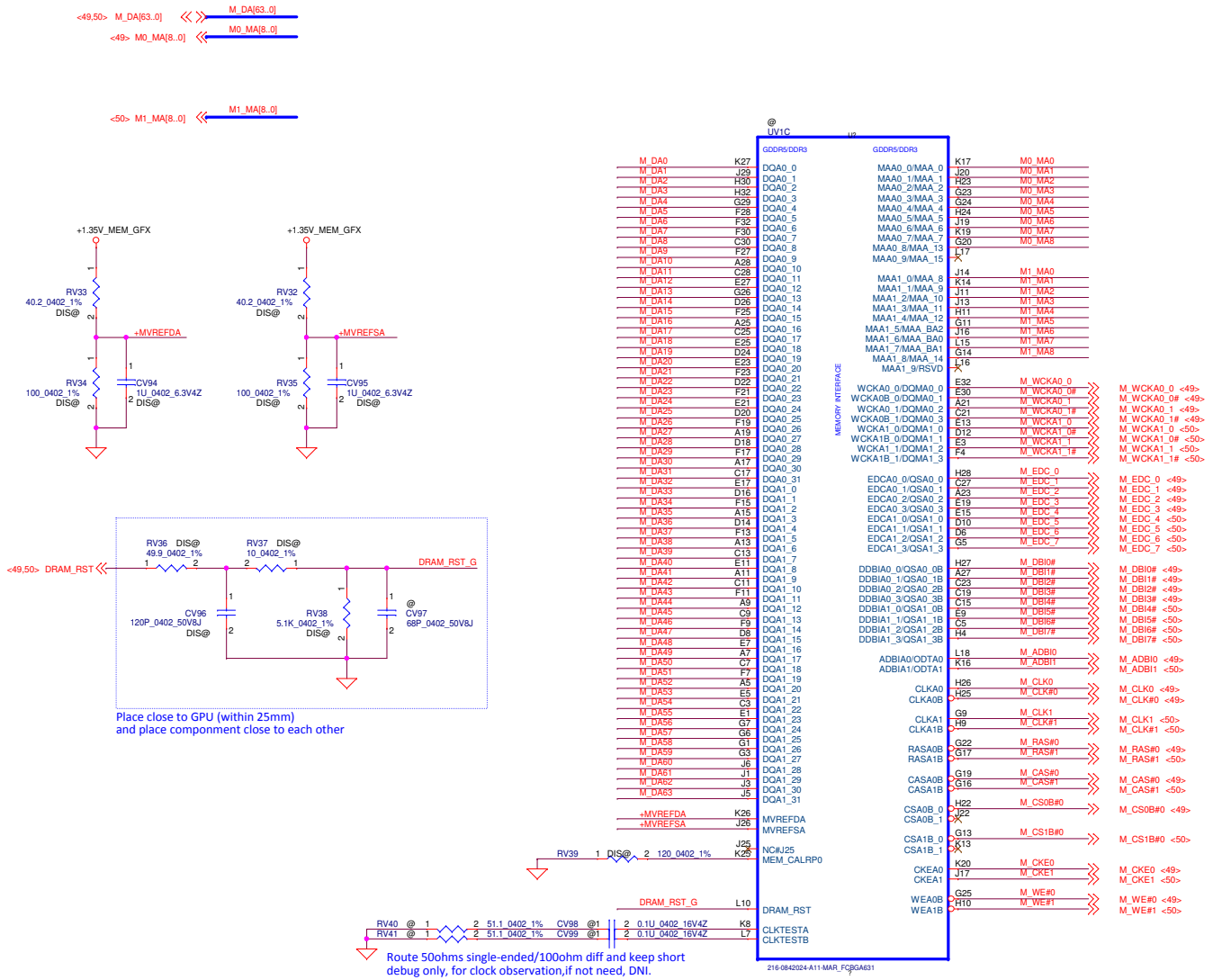
Compal Electronics, Inc.

Title: MESO_(4/5)_Power

Size: Custom | Document Number: LA-F115P | Rev: 0.1

Date: Friday, July 28, 2017 | Sheet 47 of 65

Main Func = GPU



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Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	MESO_(5/5)_MEM		
Size	Document Number		Rev
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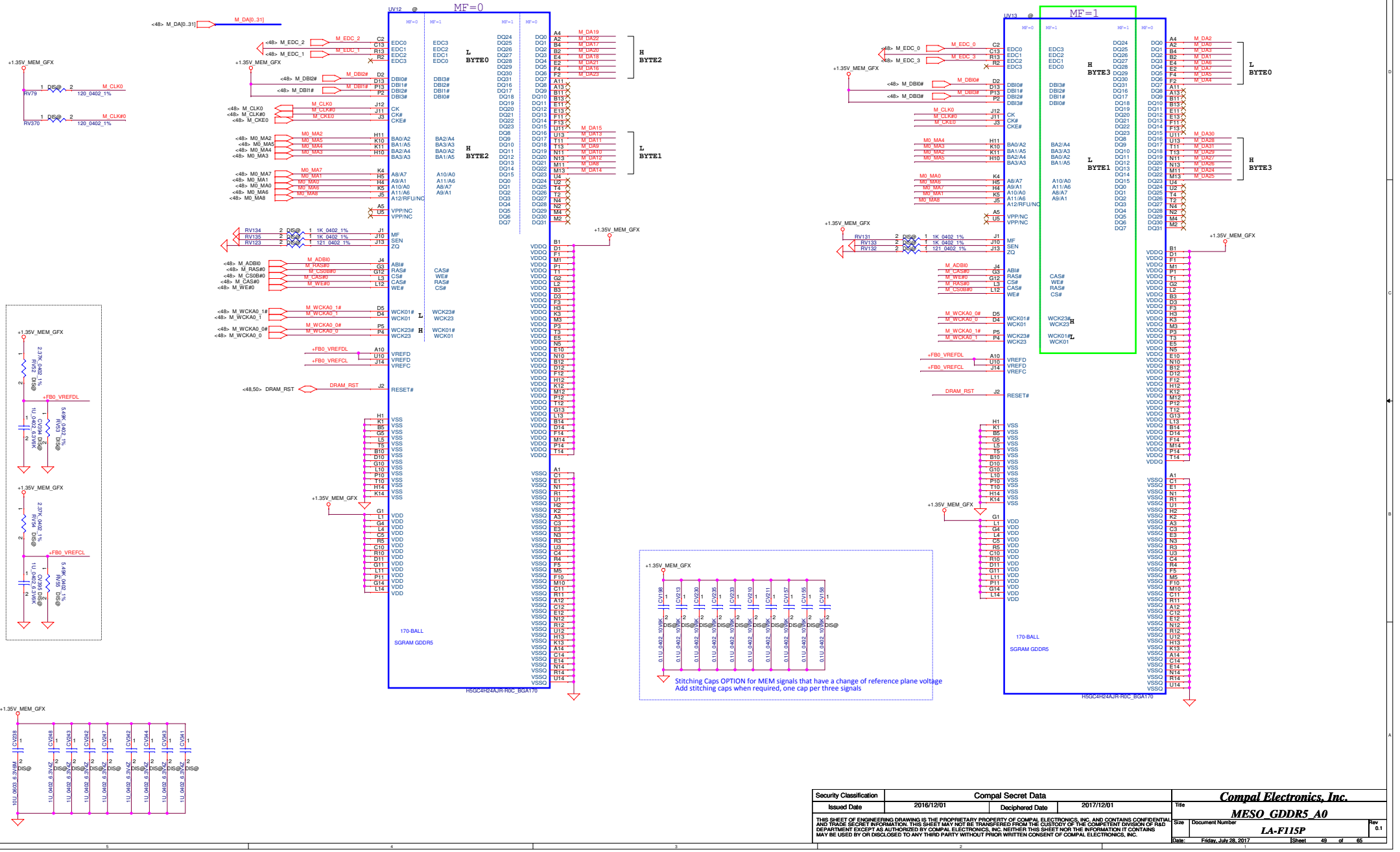
Main Func = GDDR5



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

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Compal Electronics, Inc.

Title: MESO_GDDR5_A0

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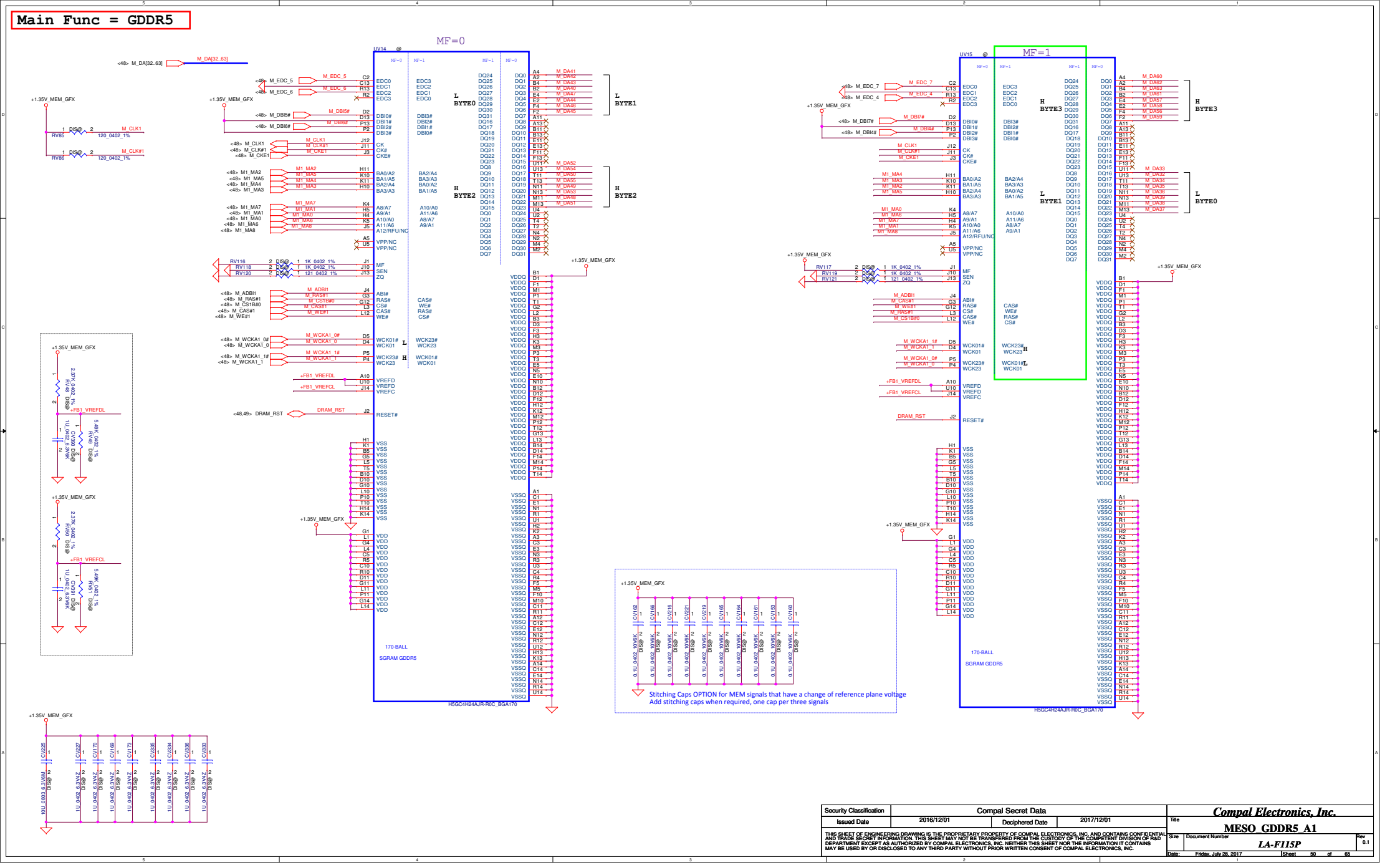
Main Func = GDDR5



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Title: MESO_GDDR5_A1

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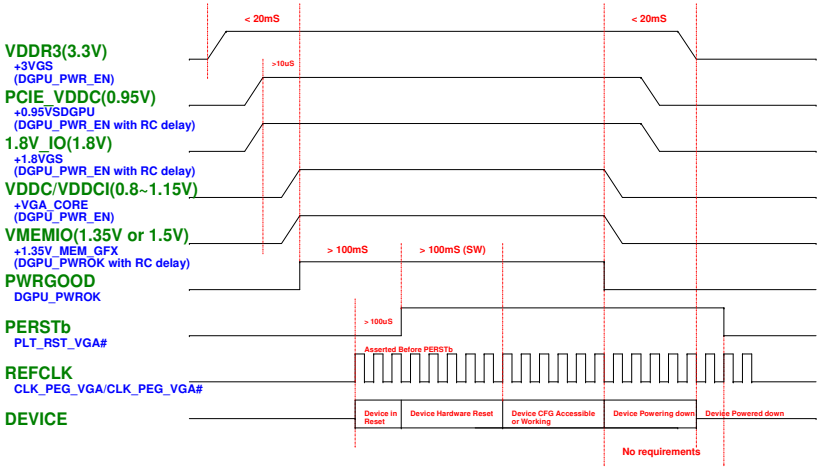
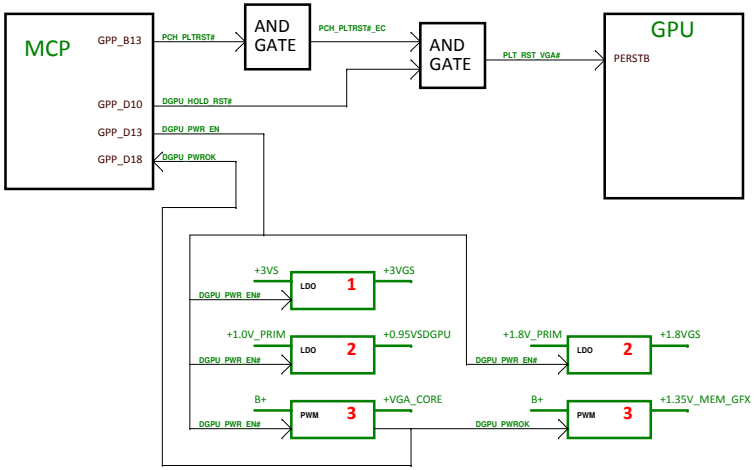
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
2. It is recommended that the 3.3-V rail ramp up first.
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ? 50 mV/µs).
5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
6. For power down, reversing the ramp-up sequence is recommended.





samsung 4G

UV12 SA000092D1L S4G_R3@ S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	UV14 SA000092D1L S4G_R3@ S IC D5 256M32 K4G80325FB-HC28 FBGA A31!
UV13 SA000092D1L S4G_R3@ S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	UV15 SA000092D1L S4G_R3@ S IC D5 256M32 K4G80325FB-HC28 FBGA A31!

samsung 2G

UV12 SA00009TT1L S2G_R3@ S IC D5 128M32 K4G41325FE-HC28 FBGA A31!	UV14 SA00009TT1L S2G_R3@ S IC D5 128M32 K4G41325FE-HC28 FBGA A31!
UV13 SA00009TT1L S2G_R3@ S IC D5 128M32 K4G41325FE-HC28 FBGA A31!	UV15 SA00009TT1L S2G_R3@ S IC D5 128M32 K4G41325FE-HC28 FBGA A31!

Hynix 4G

UV12 SA00009U11L H4G_R3@ S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!	UV14 SA00009U11L H4G_R3@ S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!
UV13 SA00009U11L H4G_R3@ S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!	UV15 SA00009U11L H4G_R3@ S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!

Hynix 2G

UV12 SA00008HQ1L H2G_R3@ S IC D5 128M32/3G H5GC4H24AJR-R0C A31!	UV14 SA00008HQ1L H2G_R3@ S IC D5 128M32/3G H5GC4H24AJR-R0C A31!
UV13 SA00008HQ1L H2G_R3@ S IC D5 128M32/3G H5GC4H24AJR-R0C A31!	UV15 SA00008HQ1L H2G_R3@ S IC D5 128M32/3G H5GC4H24AJR-R0C A31!

Micron 4G

UV12 SA00009TV1L M4G_R3@ S IC D5 256M32 MT51J256M32HF-70:A A31!	UV14 SA00009TV1L M4G_R3@ S IC D5 256M32 MT51J256M32HF-70:A A31!
UV13 SA00009TV1L M4G_R3@ S IC D5 256M32 MT51J256M32HF-70:A A31!	UV15 SA00009TV1L M4G_R3@ S IC D5 256M32 MT51J256M32HF-70:A A31!

Micron 2G

UV12 SA00009E31L M2G_R3@ S IC D5 128M32 EDW4032BABG-70-F-R A31!	UV14 SA00009E31L M2G_R3@ S IC D5 128M32 EDW4032BABG-70-F-R A31!
UV13 SA00009E31L M2G_R3@ S IC D5 128M32 EDW4032BABG-70-F-R A31!	UV15 SA00009E31L M2G_R3@ S IC D5 128M32 EDW4032BABG-70-F-R A31!

Samsung 2G	Hynix 2G	Micron 2G
RV16 2G_S@ 4.75K_0402_1% SD034475180	RV15 2G_H@ 3.4K_0402_1% SD034340180; RV16 2G_H@ 10K_0402_1% SD034100280	RV15 2G_M@ 4.75K_0402_1% SD034475180
Samsung 4G	**Hynix 4G**	**Micron 4G**
RV16 4G_S@ 4.75K_0402_1% SD034475180	RV15 4G_H@ 3.4K_0402_1% SD034340180; RV16 4G_H@ 10K_0402_1% SD034100280	RV15 4G_M@ 4.75K_0402_1% SD034475180

Table 3–21 Resistor Divider Lookup T

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

For AMD R17M-M2-50 VRAM Only

Memory ID	4Gb R3 P/N	Vendor	Configuration	Size
000	SA00009TT1L	SAMSUNG	S IC D5 128M32 K4G41325FE-HC28 FBGA A31!	2GB
110	SA00008HQ1L	Hynix	S IC D5 128M32/3G H5GC4H24AJR-R0C A31!	2GB
111	SA00009E31L	Micron	S IC D5 128M32 EDW4032BABG-70-F-R A31!	2GB

Memory ID	8Gb R3 P/N	Vendor	Configuration	Size
000	SA000092D1L	SAMSUNG	S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	4GB
110	SA00009U11L	Hynix	S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!	4GB
111	SA00009TV1L	Micron	S IC D5 256M32 MT51J256M32HF-70:A A31!	4GB

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Issued Date	2016/12/01	Deciphered Date	2017/12/01

Title	MESO_Note		
Size	Document Number LA-F115P		Rev 0.1
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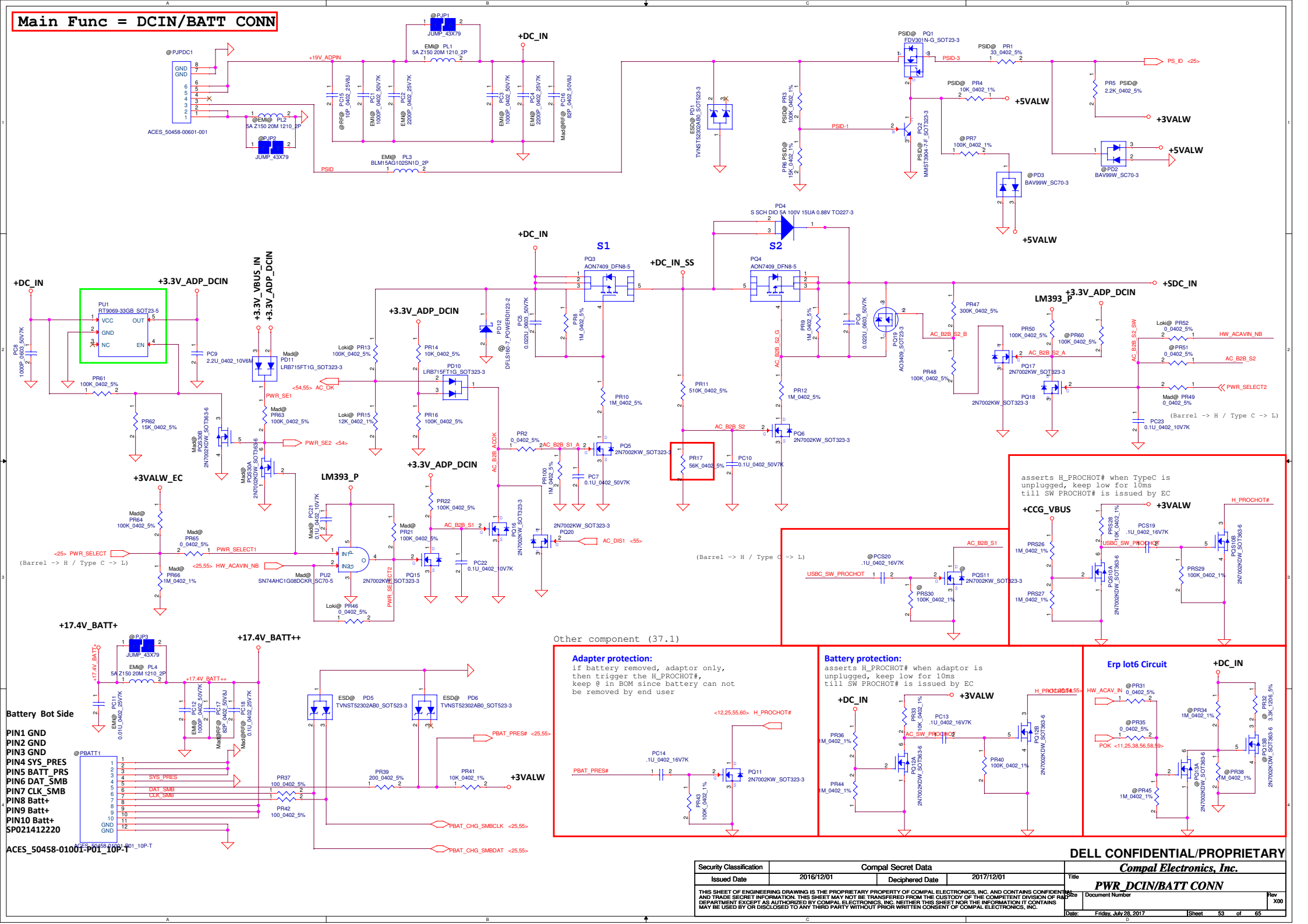
Version Change List (P. I. R. List)

Compal Electronics, Inc.		
Title: EE Change list		
Size	Document Number: LA-F115P	Rev: 0.1
Date: Friday, July 28, 2017	Sheet 52 of 65	

Main Func = DCIN/BATT CONN



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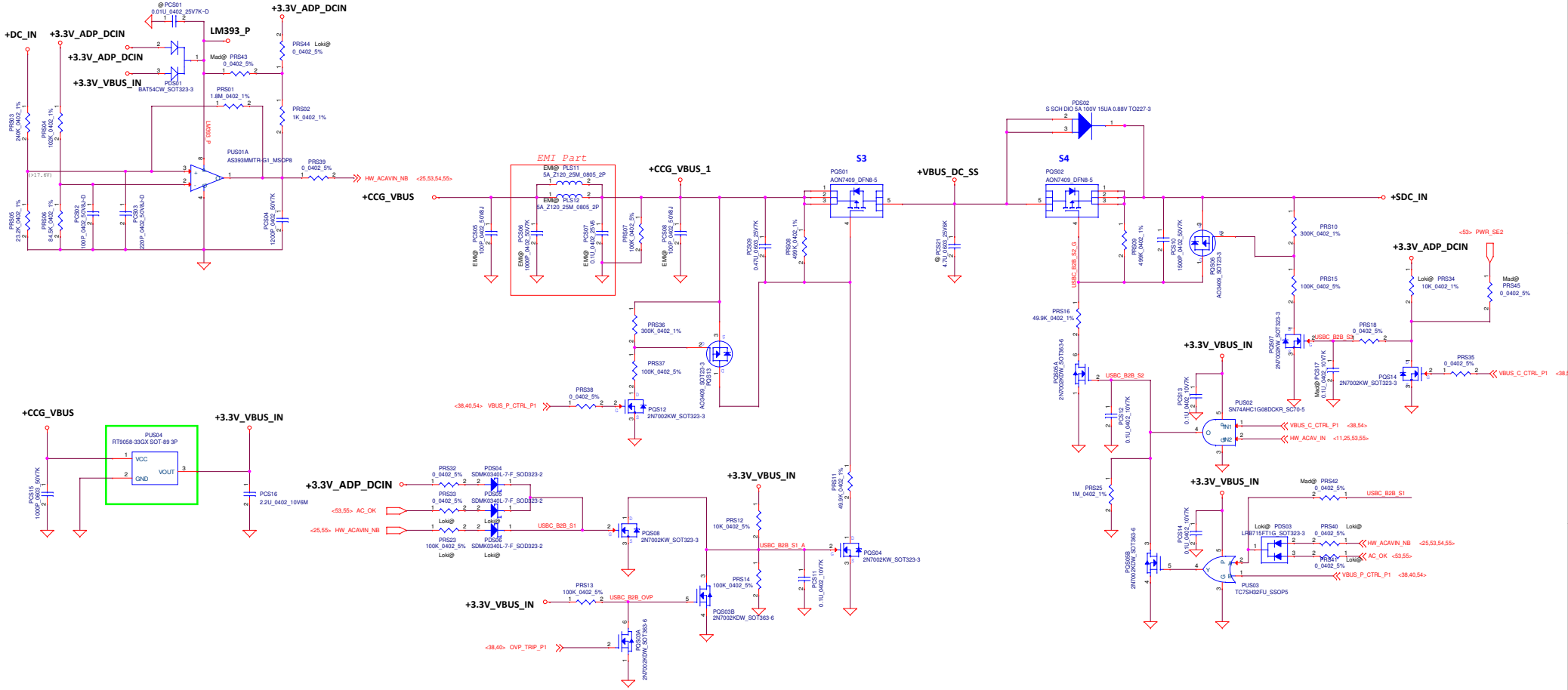
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	PWR_DCIN/BATT CONN		
Size	Document Number		Rev X00
Date: Friday, July 28, 2017	Sheet 53 of 65		

Main Func = Type-C PD Selector

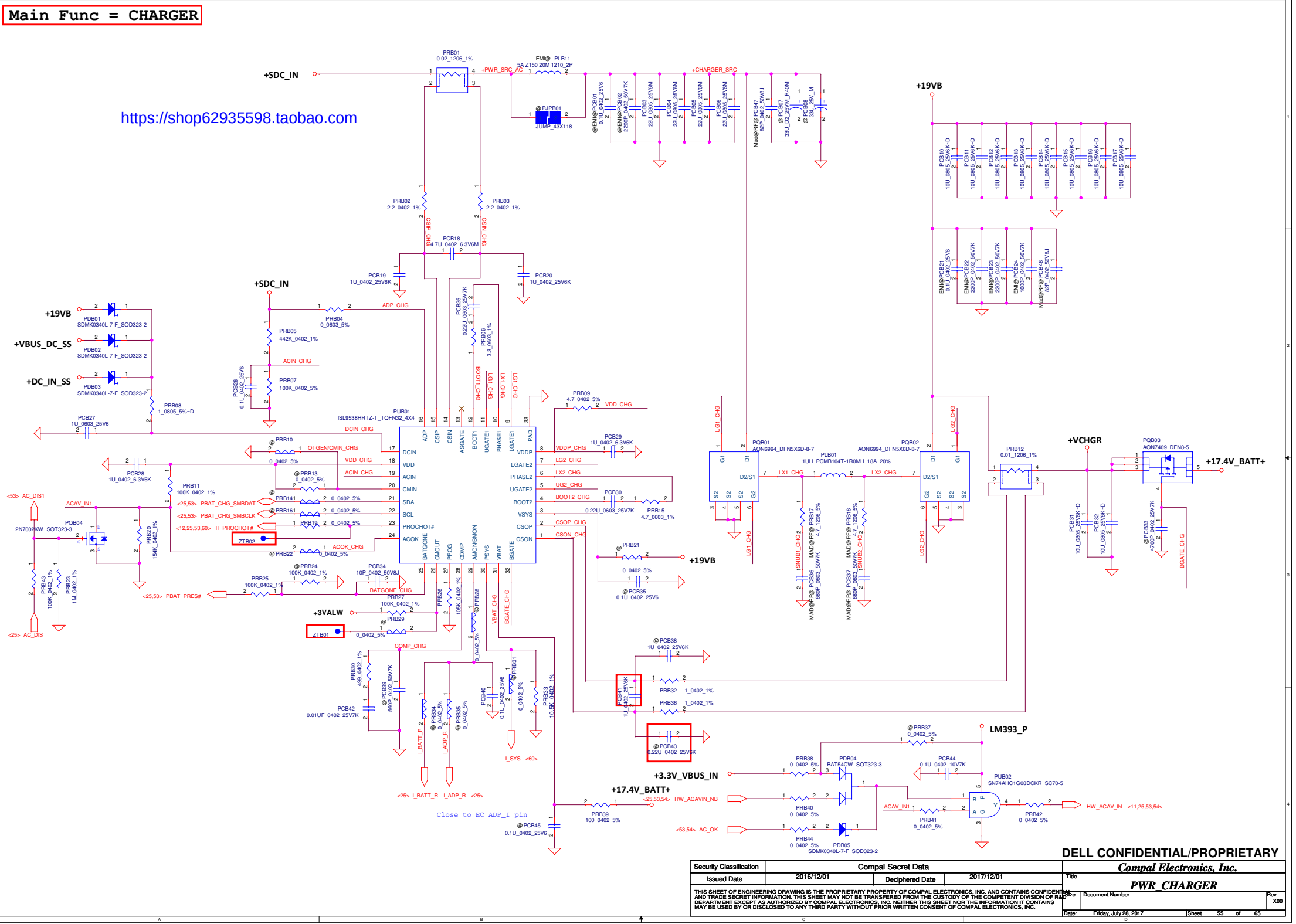
DCIN_AC_Detector



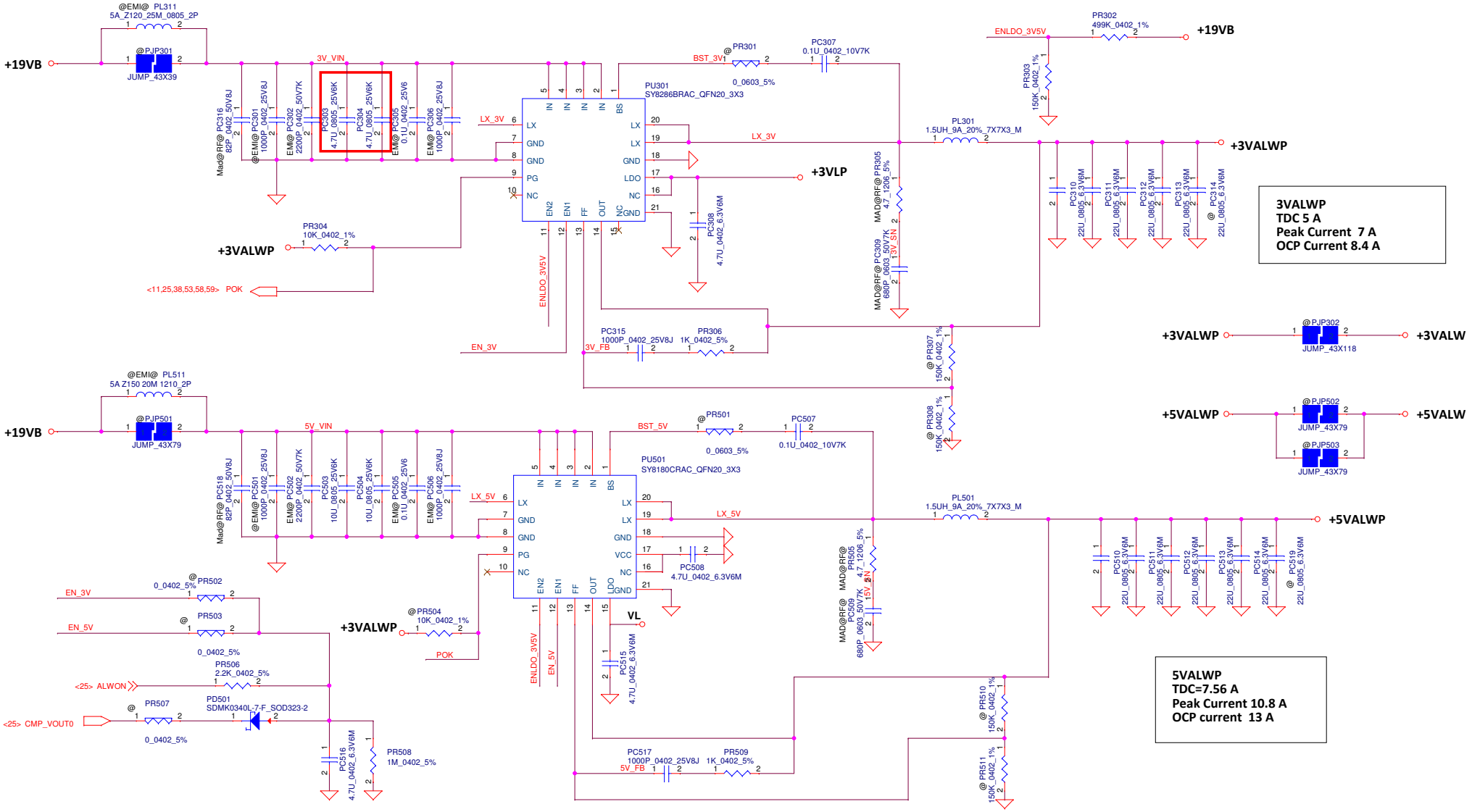
Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title: PWR_Type-C PD Selector			
Size	Document Number		Rev: X00
Date: Friday, July 28, 2017	Sheet 54 of 65		

Main Func = CHARGER



Main Func = 3.3VALWP/5VALWP



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	PWR_3.3VALWP/5VALWP		
Document Number			Rev 0.1 (X00)
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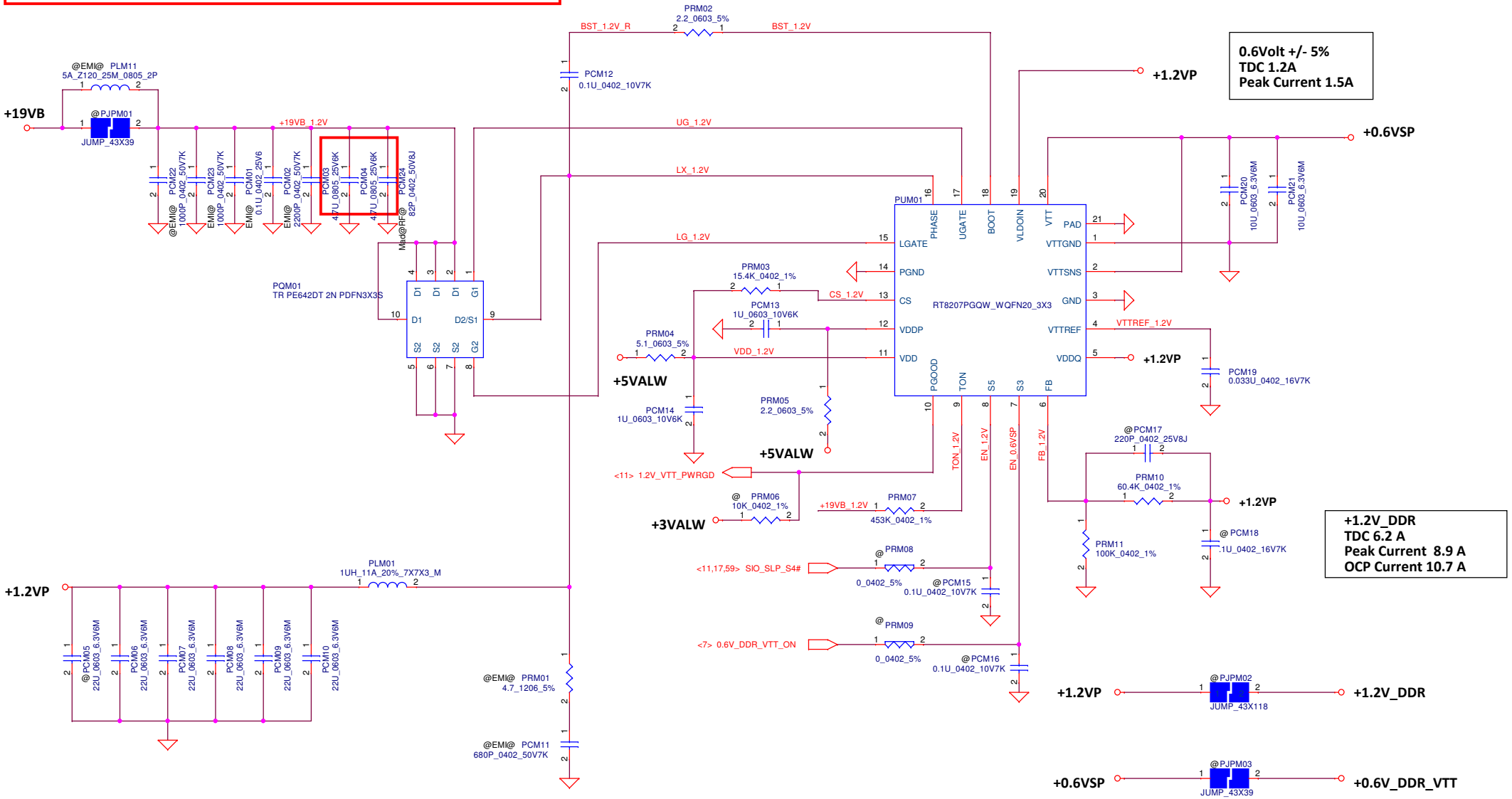
Main Func = +1.2V_DDR/+0.6V_DDR_VTT



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: PWR_+1.2V_MEN/+0.6V_DDR_VTT

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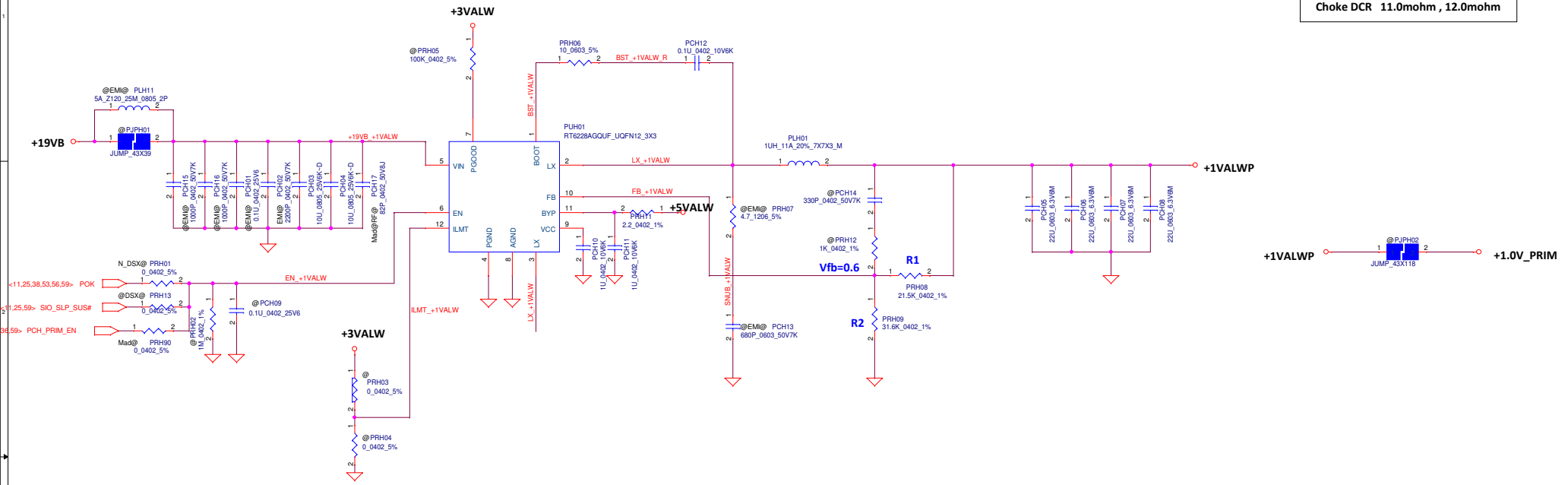
Main Func = +1VALWP

https://shop62935598.taobao.com

+1.0V_PRIM
TDC 7.6 A
Peak Current 10.8 A
OCP Current 12 A Fix by IC
TYP MAX
Choke DCR 11.0mohm , 12.0mohm



Compal Electronics, Inc.

Title: PWR_+1VALWP

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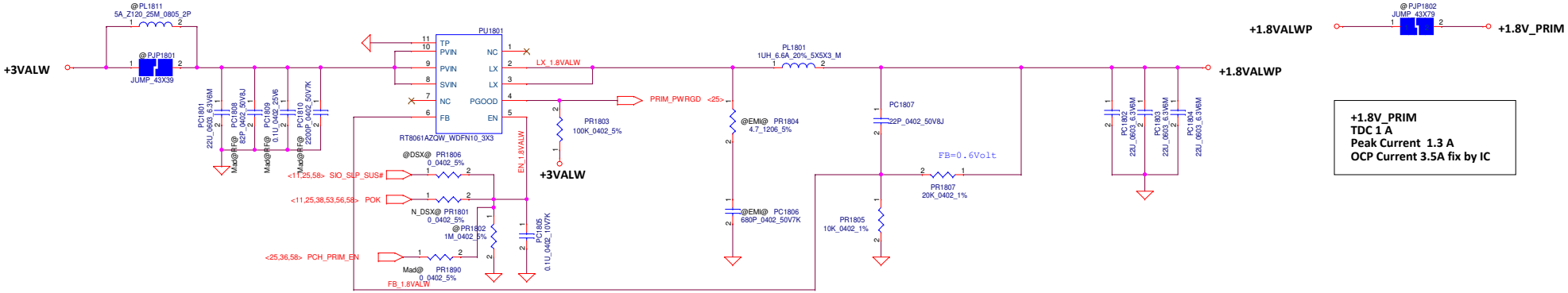
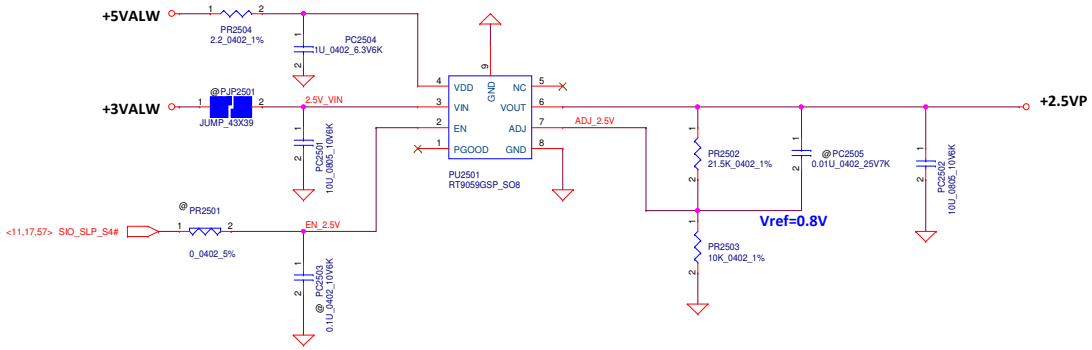
Main Func = +1.8VALWP / +2.5VP



+1.8V_PRIM
TDC 1 A
Peak Current 1.3 A
OCP Current 3.5A fix by IC



+2.5V
TDC 0.45 A
Peak Current 0.57 A

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: PWR_+1.8VALWP / +2.5VP

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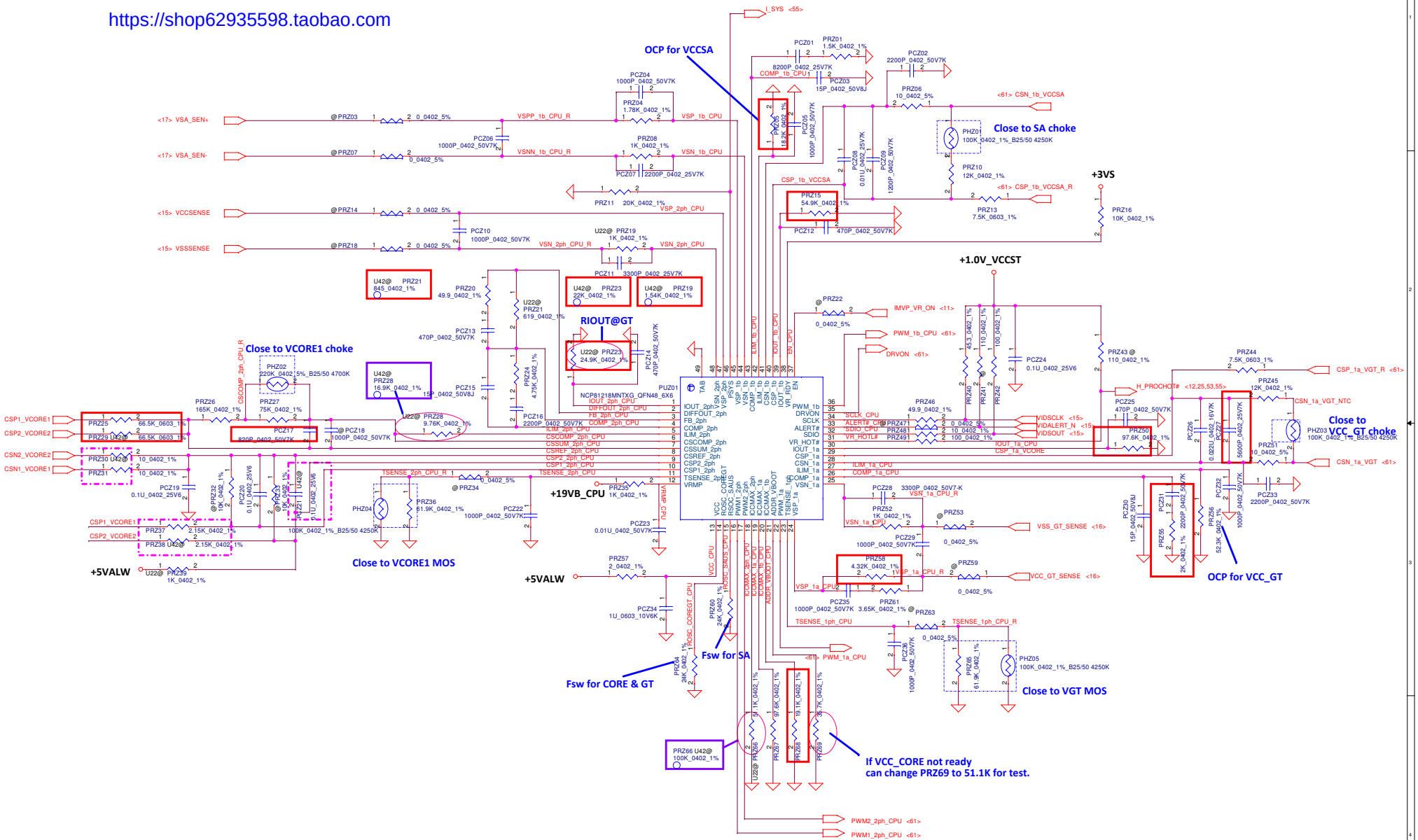
Main Func = CPU



Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	PWR_CPU		
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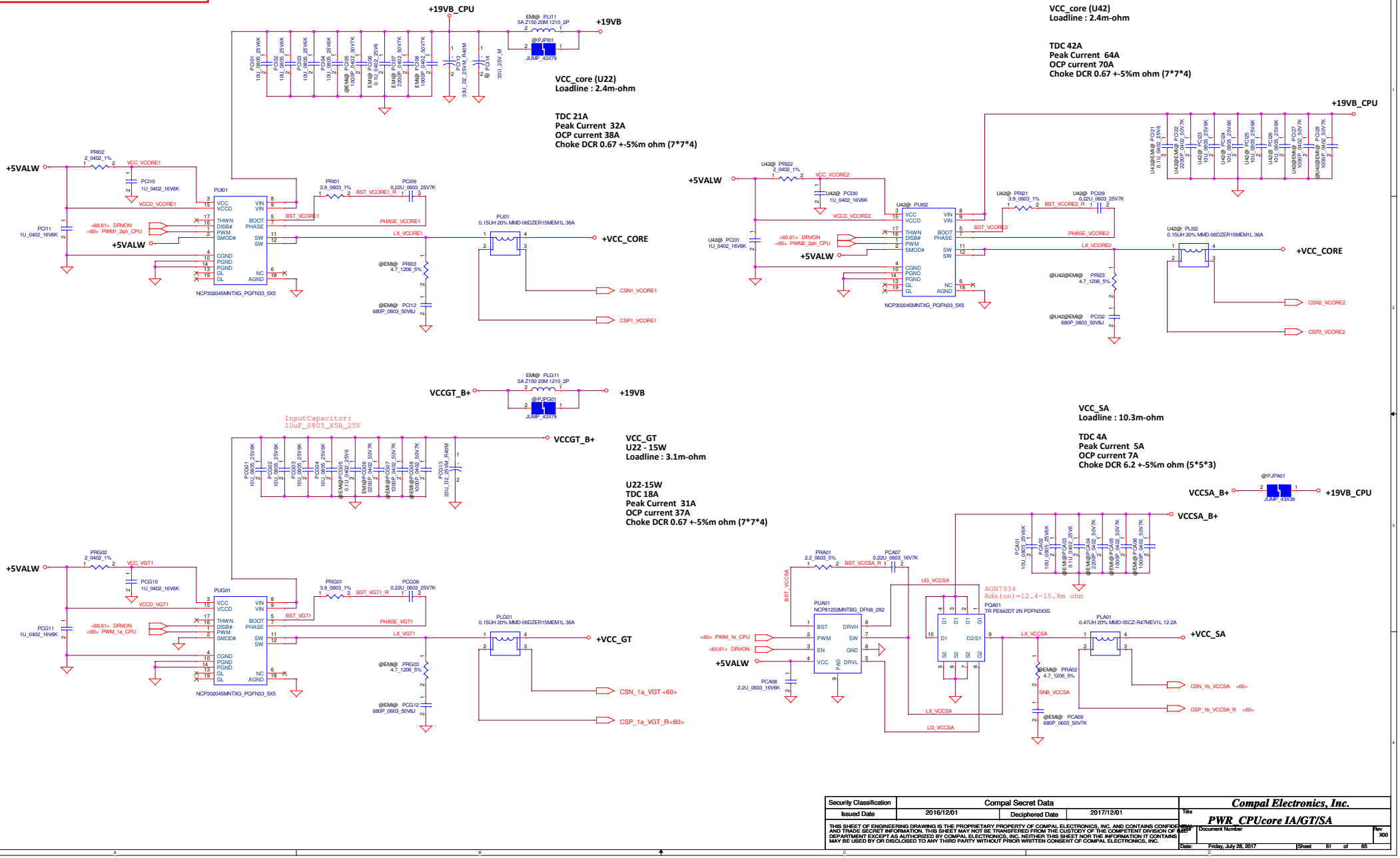
Main Func = CPUcore IA/GT/SA



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/12/01	Deciphered Date	2017/12/01
Title	PWR_CPUcore IA/GT/SA		
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Main Func = CPU/ VGA / SA MLCC

+VCC_CORE

U42@ PCI171

330U_D2_2V_Y

U42@ PCI172

330U_D2_2V_Y

Total VCORE Output Capacitor:
3 X 330uF_D2==>U42
2 X 220uF_D2==>U22
32 X 22uF_0603==>U42
20 X 22uF_0603==>U22
30 X 1uF_0201==>U42
35 X 1uF_0201==>U22

+VCC_GT

Total VCCGT Output Capacitor:
1 X 220uF_D2
35X 22uF_0603_X5R==>U22
33X 22uF_0603_X5R==>U42
4X0.47uF_0201
9X 1uF_0201

Total VCCSA Output Capacitor:
7 X 22uF_0603
7 X 1uF_0201

+VCC_CORE

+VCC_GT

+VCC_SA

+VCC_CORE

+VCC_CORE_42

+VCC_GT

+VCC_GT_42

+VCC_CORE

+VGA_CORE

For VGACORE

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: PWR_CPU / VGA / SA MLCC

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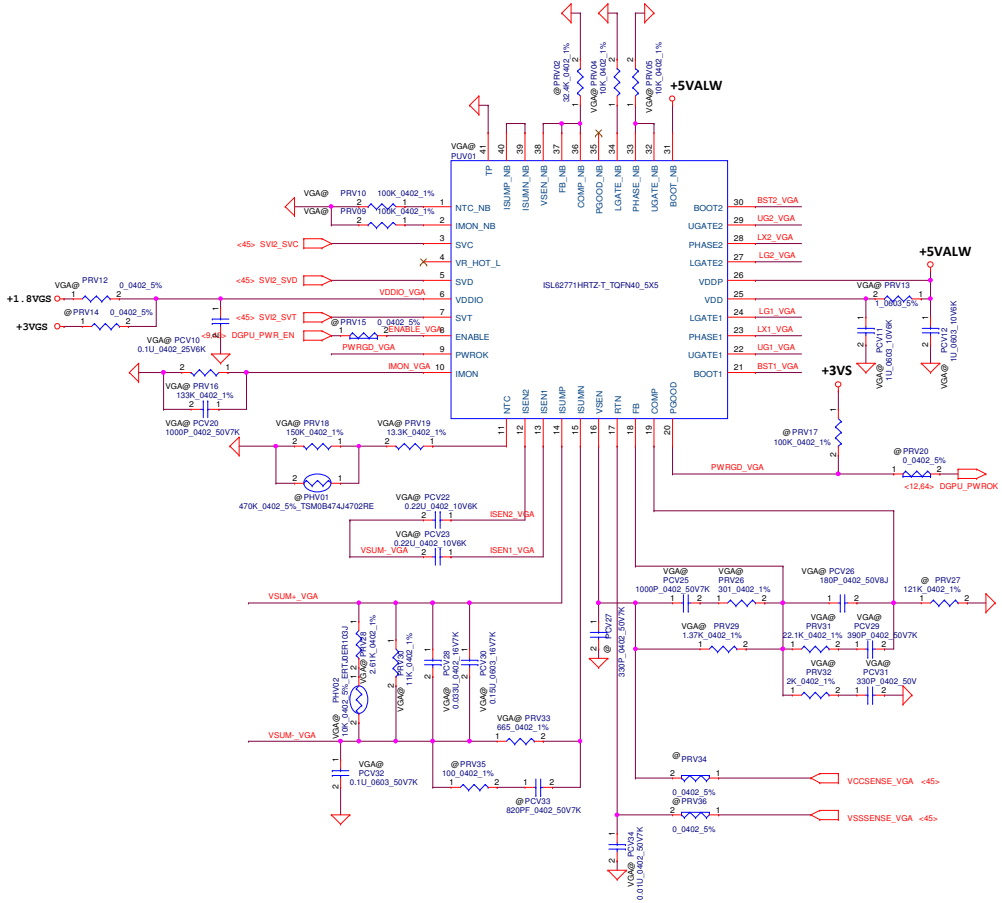
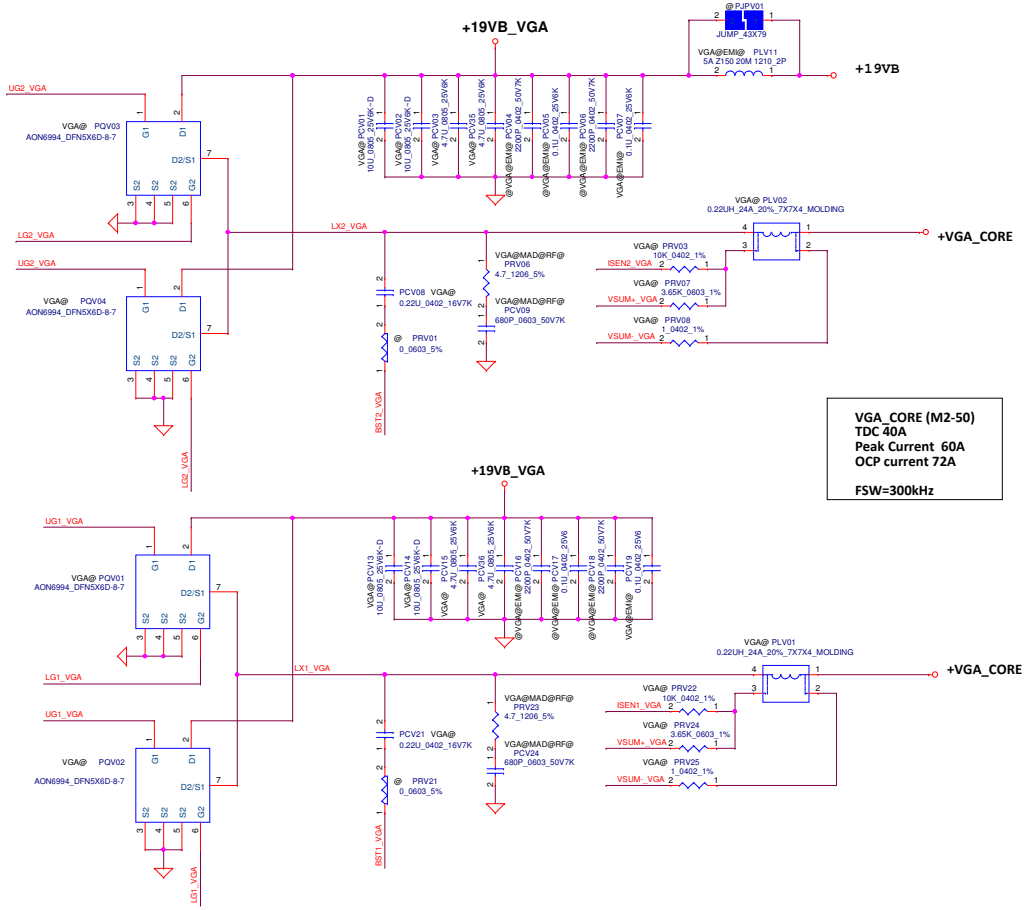
Main Func = VGA CORE





Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.

Title: **PWR_VGA_CORE**

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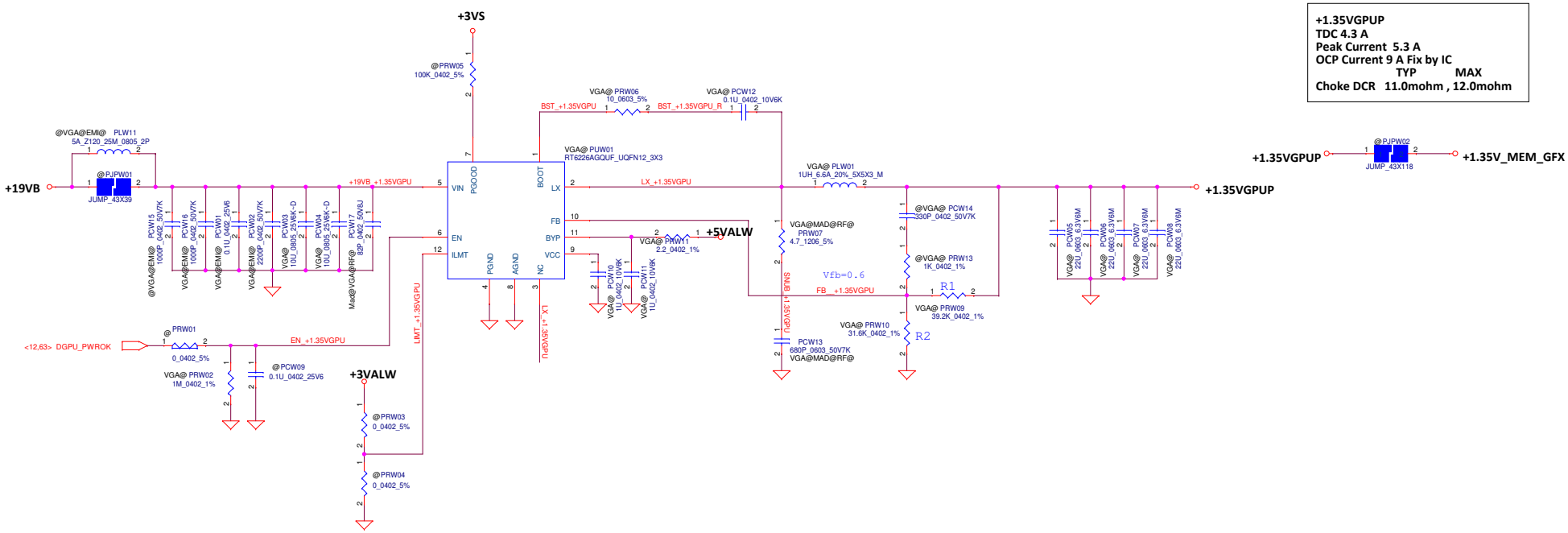
Main Func = +1.35VGPUP



+1.35VGPUP
TDC 4.3 A
Peak Current 5.3 A
OCP Current 9 A Fix by IC
TYP MAX
Choke DCR 11.0mohm , 12.0mohm

Security Classification	Compal Secret Data		
Issued Date	2016/12/01	Deciphered Date	2017/12/01

Compal Electronics, Inc.			
Title	PWR_+1.35VGPUP		
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Version Change List (P. I. R. List)

Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P51	PWR	20160321	COMPAL			0.1(X00)
2	P56	PWR	20160321	COMPAL			0.1(X00)
3							
4							
5							
6							
7							
8							

Security Classification	Compal Secret Data		
Issued Date	2015/12/22	Deciphered Date	2017/01/31

Compal Electronics, Inc.

Title: Changed-List PWR History

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